19-4971; Rev 1; 2/10

EVALUATION KIT AVAILABLE

µPMICs for Multimedia Application Processors in a 3.0mm x 2.5mm WLP

General Description

The MAX8893A/MAX8893B/MAX8893C power-management integrated circuits (PMICs) are designed for a variety of portable devices including cellular handsets. The PMICs include a high-efficiency step-down DC-DC converter, five low-dropout linear regulators (LDOs) with programmable output voltages, individual power-on/off control inputs, a load switch, and a USB high-speed switch. These devices maintain high efficiency with a low no-load supply current, and the small 3.0mm x 2.5mm WLP package makes them ideal for portable devices.

The step-down DC-DC converter utilizes a proprietary 4MHz hysteretic PWM control scheme that allows for ultra-small external components. Internal synchronous rectification improves efficiency and eliminates the external Schottky diode that is required in conventional step-down converters. Its output voltage is programmable by the I²C serial interface and output current is guaranteed up to 500mA.

LDO1, LDO4, and LDO5 offer low 45µV_{RMS} output noise and low dropout of only 100mV at 100mA. They deliver up to 300mA, 150mA, and 200mA continuous output currents, respectively. LDO2 and LDO3 each deliver 300mA continuous output current with very low ground current. All LDO output voltages are programmable by the I²C serial interface. Three standard versions of the PMIC are available with different LDO default startup voltages (see Table 1).

The MAX8893A/MAX8893B/MAX8893C are available in a 3.0mm x 2.5mm, 30-bump WLP package.

Applications

Cellular Handsets

Smartphones and PDAs

Typical Operating Circuit appears at end of data sheet.

Features

- **High-Efficiency Step-Down Converter**
  - **Guaranteed 500mA Output Current**
  - **Up to 4MHz Switching Frequency**
  - **Programmable Output Voltage from 0.8V to 2.4V**
  - **Dynamic Voltage Scaling with Programmable Ramp Rate**
- **Three Low-Noise LDOs with Programmable Output Voltages**
- **Two Low Supply Current LDOs with Programmable Output Voltages**
- **Low On-Resistance Load Switch**
- **USB High-Speed Switch with ±15kV ESD**
- **Individual Enable Control for All Regulators and Switches**
- **I²C Serial Interface**
- **Overcurrent and Thermal Protection for All LDOs**
- **3.0mm x 2.5mm x 0.64mm, 30-Bump WLP**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX8893AEWV+	-40°C to +85°C	30-Bump WLP (3.0mm x 2.5mm)
MAX8893BEWV+	-40°C to +85°C	30-Bump WLP (3.0mm x 2.5mm)
MAX8893CEWV+	-40°C to +85°C	30-Bump WLP (3.0mm x 2.5mm)

+Denotes a lead(Pb)-free/RoHS-compliant package.

µPMICs for Multimedia Application Processors in a 3.0mm x 2.5mm WLP

ABSOLUTE MAXIMUM RATINGS

IN1, IN2, BATT, COM1, COM2 to AGND ..... -0.3V to +6.0V
BUCK, LS, ENLS, ENBUCK, ENLDO1, ENLDO2, ENLDO3, ENLDO45, REFBP, LDO2, LDO3, SCL, SDA, ENUSB, CB, NC1, NC2, NO1, NO2 to AGND ..... -0.3V to (V_{BATT} + 0.3V)
LDO1, LDO4, LDO5 to AGND ..... -0.3V to (V_{IN2} + 0.3V)
PGND to AGND ..... -0.3V to +0.3V
LX Current ..... 1.5A_{RMS}
LX to AGND (Note 1) ..... -0.3V to (V_{IN1} + 0.3V)

Continuous Power Dissipation (T_A = +70°C)
30-Bump, 3.0mm x 2.5mm WLP (derate 20.0mW/°C above +70°C) 1600mW
Junction-to-Ambient Thermal Resistance (θ_{JA}) (Note 2) ..... 50°C/W
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Bump Temperature (soldering)
Infrared (15s) ..... +200°C
Vapor Phase (20s) ..... +215°C

Note 1: LX has internal clap diodes to PGND and IN1. Applications that forward bias these diodes should take care not to exceed the IC's package-dissipation limits.

Note 2: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(*Typical Operating Circuit*, V_{IN} = 3.7V, C_{BATT} = C_{IN1} = C_{IN2} = 2.2µF, C_{REFBP} = 0.1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 3, 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Supply Range		2.7		5.5	V
Shutdown Supply Current	V_{CB} = 0V or V_{IN}, $V_{\overline{ENUSB}}$ = V_{IN}, V_{ENLS} = V_{ENBUCK} = V_{ENLDO1} = V_{ENLDO2} = V_{ENLDO3} = $V_{ENLDO45}$ = 0V		0.6	5	µA
No-Load Supply Current	No load on BUCK, LDO1, LDO2, LDO3, LDO4, and LDO5, $V_{\overline{ENUSB}}$ = 0V, V_{ENLS} = V_{IN}		160	200	µA
Light-Load Supply Current	BUCK on with 500µA load, all LDOs on with no load, $V_{\overline{ENUSB}}$ = 0V, V_{ENLS} = V_{IN}		315		µA
UNDERVOLTAGE LOCKOUT					
Undervoltage Lockout (Note 5)	$V_{IN\_}$ rising	2.70	2.85	3.05	V
	$V_{IN\_}$ falling		2.35	2.55	
THERMAL SHUTDOWN					
Thermal Shutdown Threshold	T_A rising		160		°C
Thermal Shutdown Hysteresis			10		°C
REFERENCE					
Reference Bypass Output Voltage		0.786	0.800	0.814	V
REF Supply Rejection	2.7V ≤ V_{IN} ≤ 5.5V		0.2		mV/V
LOGIC AND CONTROL INPUTS					
Input Low Level	ENLS, ENBUCK, ENLDO1, ENLDO2, ENLDO3, ENLDO45, $\overline{ENUSB}$, SDA, SCL, 2.7V ≤ V_{IN} ≤ 5.5V			0.4	V
Input High Level	ENLS, ENBUCK, ENLDO1, ENLDO2, ENLDO3, ENLDO45, $\overline{ENUSB}$, SDA, SCL, 2.7V ≤ V_{IN} ≤ 5.5V	1.4			V

ELECTRICAL CHARACTERISTICS (continued)

(*Typical Operating Circuit*, V_{IN} = 3.7V, C_{BATT} = C_{IN1} = C_{IN2} = 2.2µF, C_{REFBP} = 0.1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Logic Input Current	SDA, SCL, 0V < V_{IN} < 5.5V	T_A = +25°C	-1		+1	µA
		T_A = +85°C		0.1		
$\overline{ENUSB}$ Pullup Resistor to BATT			400	800	1600	kΩ
ENLS, ENBUCK, ENLDO1, ENLDO2, ENLDO3, ENLDO45, Pulldown Resistor to AGND			400	800	1600	kΩ
STEP-DOWN DC-DC CONVERTER (BUCK)						
Supply Current	I_{LOAD} = 0A, no switching			25		µA
Programmable Output Voltage	I_{LOAD} = 100mA, programmable output voltage 0.8V to 2.4V in 100mV steps		0.776	0.800	0.824	V
				0.90		
			0.97	1.00	1.03	
				1.10		
				1.20		
				1.30		
				1.40		
				1.50		
				1.60		
				1.70		
				1.80		
				1.90		
				2.00		
				2.10		
				2.20		
			2.231	2.300	2.369	
			2.328	2.400	2.472	
Output-Voltage Line Regulation	V_{IN} = 2.7V to 5.5V			0.3		%/V
LX Leakage Current	V_{LX} = 0V or 5.5V	T_A = +25°C	-1		+1	µA
		T_A = +85°C		0.1		
Current Limit	p-MOSFET switch		600	990	1500	mA
	n-MOSFET rectifier		400	700	1300	
On-Resistance	p-MOSFET switch, I_{LX} = -40mA			0.65		Ω
	n-MOSFET rectifier, I_{LX} = 40mA			0.4		
Rectifier Off Current Threshold	I_{LXOFF}			30		mA
Minimum On- and Off-Times	t_{ON}, t_{OFF}			70		ns
Shutdown Output Resistance	BUCK_ADEN = 1, V_{ENBUCK} = 0V			300		Ω

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ELECTRICAL CHARACTERISTICS (continued)

(*Typical Operating Circuit*, V_{IN} = 3.7V, C_{BATT} = C_{IN1} = C_{IN2} = 2.2µF, C_{REFBP} = 0.1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 3, 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
LDO1					
Input Voltage Range		2.7		5.5	V
Programmable Output Voltage	I_{LOAD} = 25mA, programmable output voltage 1.6V to 3.3V in 100mV steps	1.552	1.600	1.648	V
			1.70		
			1.80		
			1.90		
			2.00		
			2.10		
			2.20		
			2.30		
			2.40		
			2.50		
			2.60		
			2.70		
			2.80		
			2.90		
		2.910	3.000	3.090	
			3.1		
			3.2		
		3.201	3.300	3.399	
Output Voltage Accuracy	V_{IN} = 5.5V with I_{LOAD} = 1mA, and V_{IN} = 3.2V with I_{LOAD} = 300mA (MAX8893A)	2.716	2.800	2.884	V
	V_{IN} = 5.5V with I_{LOAD} = 1mA, and V_{IN} = 3.0V with I_{LOAD} = 300mA (MAX8893B)	2.522	2.600	2.678	
	V_{IN} = 5.5V with I_{LOAD} = 1mA, and V_{IN} = 2.7V with I_{LOAD} = 300mA (MAX8893C)	1.746	1.800	1.854	
Output Current				300	mA
Current Limit	V_{LDO1} = 0V		550		mA
Dropout Voltage	I_{LOAD} = 200mA, T_A = +25°C		200		mV
Load Regulation	1mA < I_{LOAD} < 300mA, V_{ENLDO1} = V_{BATT}		25		mV
Power-Supply Rejection $\Delta V_{LDO1}/\Delta V_{IN2}$	10Hz to 10kHz, C_{LDO1} = 1µF, I_{LOAD} = 30mA		75		dB
Output Noise Voltage	100Hz to 100kHz, C_{LDO1} = 1µF, I_{LOAD} = 30mA		45		μV_{RMS}
Output Capacitor for Stable Operation (Note 6)	0mA < I_{LOAD} < 300mA	1.4	2.2		µF
	0mA < I_{LOAD} < 150mA	0.7	1.0		
Ground Current	I_{LOAD} = 500µA		21		µA
Startup Time from Shutdown	C_{LDO1} = 2.2µF, I_{LOAD} = 300mA		40		µs
Shutdown Output Resistance	LDO1_ADEN = 1, V_{ENLDO1} = 0V		300		Ω

ELECTRICAL CHARACTERISTICS (continued)

(*Typical Operating Circuit*, V_{IN} = 3.7V, C_{BATT} = C_{IN1} = C_{IN2} = 2.2µF, C_{REFBP} = 0.1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 3, 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
LDO2					
Input Voltage Range		2.7		5.5	V
Programmable Output Voltage	I_{LOAD} = 25mA, programmable output voltage 1.2V to 3.3V in 100mV steps	1.164	1.200	1.236	V
			1.30		
			1.40		
			1.50		
			1.60		
			1.70		
			1.80		
			1.90		
			2.00		
			2.10		
		2.134	2.200	2.266	
			2.30		
			2.40		
			2.50		
			2.60		
			2.70		
			2.80		
			2.90		
			3.00		
			3.10		
			3.20		
		3.201	3.300	3.399	
Output Voltage Accuracy	V_{IN} = 5.5V with I_{LOAD} = 1mA, and V_{IN} = 3.0V with I_{LOAD} = 300mA	2.522	2.600	2.678	V
Output Current				300	mA
Current Limit	V_{LDO2} = 0V		550		mA
Dropout Voltage	I_{LOAD} = 200mA, T_A = +25°C		200		mV
Load Regulation	1mA < I_{LOAD} < 300mA, V_{ENLDO2} = V_{BATT}		25		mV
Power-Supply Rejection $\Delta V_{LDO2}/\Delta V_{BATT}$	10Hz to 10kHz, C_{LDO2} = 1µF, I_{LOAD} = 30mA		60		dB
Output Noise Voltage	100Hz to 100kHz, C_{LDO2} = 1µF, I_{LOAD} = 30mA		80		μV_{RMS}
Output Capacitor for Stable Operation (Note 6)	0mA < I_{LOAD} < 300mA	1.4	2.2		µF
	0mA < I_{LOAD} < 150mA	0.7	1.0		
Ground Current	I_{LOAD} = 500µA		21		µA
Startup Time from Shutdown	C_{LDO2} = 1µF, I_{LOAD} = 300mA		40		µs
Shutdown Output Resistance	LDO2_ADEN = 1, V_{ENLDO2} = 0V		300		Ω

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ELECTRICAL CHARACTERISTICS (continued)

(*Typical Operating Circuit*, V_{IN} = 3.7V, C_{BATT} = C_{IN1} = C_{IN2} = 2.2µF, C_{REFBP} = 0.1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 3, 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
LDO3					
Input Voltage Range		2.7		5.5	V
Programmable Output Voltage	I_{LOAD} = 25mA, programmable output voltage 1.6V to 3.3V in 100mV steps	1.552	1.600	1.648	V
			1.70		
			1.80		
			1.90		
			2.00		
			2.10		
			2.20		
			2.30		
			2.40		
			2.50		
			2.60		
			2.70		
			2.80		
			2.90		
		2.910	3.000	3.090	
			3.10		
			3.20		
		3.201	3.300	3.399	
Output Voltage Accuracy	V_{IN} = 5.5V with I_{LOAD} = 1mA, and V_{IN} = 3.7V with I_{LOAD} = 300mA	3.201	3.300	3.399	V
Output Current				300	mA
Current Limit	V_{LDO3} = 0V		550		mA
Dropout Voltage	I_{LOAD} = 200mA, T_A = +25°C		200		mV
Load Regulation	1mA < I_{LOAD} < 300mA, V_{ENLDO3} = V_{BATT}		25		mV
Power-Supply Rejection $\Delta V_{LDO3}/\Delta V_{BATT}$	10Hz to 10kHz, C_{LDO3} = 1µF, I_{LOAD} = 30mA		60		dB
Output Noise Voltage	100Hz to 100kHz, C_{LDO3} = 1µF, I_{LOAD} = 30mA		80		μV_{RMS}
Output Capacitor for Stable Operation (Note 6)	0mA < I_{LOAD} < 300mA	1.4	2.2		µF
	0mA < I_{LOAD} < 150mA	0.7	1.0		
Ground Current	I_{LOAD} = 500µA		21		µA
Startup Time from Shutdown	C_{LDO3} = 2.2µF, I_{LOAD} = 300mA		40		µs
Shutdown Output Resistance	LDO3_ADEN = 1, V_{ENLDO3} = 0V		300		Ω

ELECTRICAL CHARACTERISTICS (continued)

(*Typical Operating Circuit*, V_{IN} = 3.7V, C_{BATT} = C_{IN1} = C_{IN2} = 2.2µF, C_{REFBP} = 0.1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 3, 4)

LDO4					
Input Voltage Range		2.7		5.5	V
Programmable Output Voltage	I_{LOAD} = 25mA, programmable output voltage 0.8V to 3.3V in 100mV steps	0.776	0.800	0.824	V
			0.90		
			1.00		
			1.10		
			1.20		
			1.30		
		1.358	1.400	1.442	
			1.50		
			1.60		
			1.70		
			1.80		
			1.90		
			2.00		
			2.10		
			2.20		
			2.30		
			2.40		
			2.50		
			2.60		
			2.70		
			2.80		
			2.90		
			3.00		
			3.10		
			3.20		
		3.201	3.300	3.399	
Output Voltage Accuracy	V_{IN} = 5.5V with I_{LOAD}=1mA, and V_{IN} = 3.4V with I_{LOAD} = 150mA (MAX8893A)	2.910	3.000	3.090	V
	V_{IN} = 5.5V with I_{LOAD} = 1mA, and V_{IN} = 3.7V with I_{LOAD} = 150mA (MAX8893B/MAX8893C)	3.201	3.300	3.399	
Output Current				150	mA
Current Limit	V_{LDO4} = 0V		360		mA
Dropout Voltage	I_{LOAD} = 100mA		100		mV
Load Regulation	1mA < I_{LOAD} < 150mA, V_{ENLDO4} = V_{BATT}		25		mV
Power-Supply Rejection $\Delta V_{LDO4}/\Delta V_{IN2}$	10Hz to 10kHz, C_{LDO4} = 1µF, I_{LOAD} = 30mA		75		dB
Output Noise Voltage	100Hz to 100kHz, C_{LDO4} = 1µF, I_{LOAD} = 30mA		45		μV_{RMS}
Output Capacitor for Stable Operation	0mA < I_{LOAD} < 150mA (Note 6)	0.7	1.0		µF

ELECTRICAL CHARACTERISTICS (continued)

(*Typical Operating Circuit*, V_{IN} = 3.7V, C_{BATT} = C_{IN1} = C_{IN2} = 2.2μF, C_{REFBP} = 0.1μF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 3, 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Ground Current	I_{LOAD} = 500μA		21		μA
Startup Time from Shutdown	C_{LDO4} = 1.0μF, I_{LOAD} = 150mA		40		μs
Shutdown Output Resistance	LDO4_ADEN = 1, V_{ENLDO4} = 0V		300		Ω
LDO5					
Input Voltage Range		2.7		5.5	V
Programmable Output Voltage	I_{LOAD} = 100mA, programmable output voltage 0.8V to 3.3V in 100mV steps	0.776	0.800	0.824	V
			0.90		
			1.00		
			1.10		
			1.20		
			1.30		
		1.358	1.400	1.442	
			1.50		
			1.60		
			1.70		
			1.80		
			1.90		
			2.00		
			2.10		
			2.20		
			2.30		
			2.40		
			2.50		
			2.60		
			2.70		
			2.80		
			2.90		
			3.00		
			3.10		
			3.20		
		3.201	3.300	3.399	
Output Voltage Accuracy	V_{IN} = 5.5V with I_{LOAD} = 1mA, and V_{IN} = 3.4V with I_{LOAD} = 150mA (MAX8893A)	0.970	1.000	1.030	V
	V_{IN} = 5.5V with I_{LOAD} = 1mA, and V_{IN} = 3.4V with I_{LOAD} = 150mA (MAX8893B)	2.716	2.800	2.884	
	V_{IN} = 5.5V with I_{LOAD} = 1mA, and V_{IN} = 3.4V with I_{LOAD} = 150mA (MAX8893C)	2.910	3.000	3.090	
Output Current				200	mA
Current Limit	V_{LDO5} = 0V		460		mA
Dropout Voltage	I_{LOAD} = 100mA		100		mV

ELECTRICAL CHARACTERISTICS (continued)

(*Typical Operating Circuit*, V_{IN} = 3.7V, C_{BATT} = C_{IN1} = C_{IN2} = 2.2µF, C_{REFBP} = 0.1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Load Regulation	1mA < I_{LOAD} < 150mA V_{ENLDO5} = V_{BATT}			25		mV
Power-Supply Rejection $\Delta V_{LDO5}/\Delta V_{IN2}$	10Hz to 10kHz, C_{LDO5} = 1µF, I_{LOAD} = 30mA			75		dB
Output Noise Voltage	100Hz to 100kHz, C_{LDO5} = 1µF, I_{LOAD} = 30mA			45		μV_{RMS}
Output Capacitor for Stable Operation (Note 6)	0mA < I_{LOAD} < 200mA		1.4	2.2		µF
	0mA < I_{LOAD} < 150mA		0.7	1.0		
Ground Current	I_{LOAD} = 500µA			21		µA
Startup Time from Shutdown	C_{LDO5} = 2.2µF, I_{LOAD} = 200mA			40		µs
Shutdown Output Resistance	LDO5_ADEN = 1, V_{ENLDO5} = 0V			300		Ω
USB HIGH-SPEED SWITCH						
Operating Power-Supply Range			2.7		5.5	V
Supply Current	$V_{\overline{ENUSB}}$ = 0V, V_{CB} = 0V or V_{BATT}	V_{BATT} = 3.0V		0.6		µA
		V_{BATT} = 5.5V		3		
Fault Protection Trip Threshold (V_{FP})	COM_ only, T_A = +25°C		V_{IN} + 0.6	V_{IN} + 0.8	V_{IN} + 1.0	V
On-Resistance (R_{ON})	$V_{COM\_}$ = 0V to V_{BATT}			5	10	Ω
	$V_{COM\_}$ = 3.6V, V_{BATT} = 3.0V			5.5		
On-Resistance Match Between Channels (ΔR_{ON})	V_{BATT} = 3.0V, $V_{COM\_}$ = 2V (Note 7)			0.1	1	Ω
On-Resistance Flatness (R_{FLAT})	V_{BATT} = 3.0V, $V_{COM\_}$ = 0V to V_{IN} (Note 8)			0.1		Ω
Off-Leakage Current ($I_{COM\_(OFF)}$)	V_{BATT} = 4.5V, $V_{COM\_}$ = 0V or 4.5V, $V_{NO\_}$, $V_{NC\_}$ = 4.5V or 0V		-250		+250	nA
	V_{BATT} = 5.5V, $V_{COM\_}$ = 0V or 5.5V, $V_{NO\_}$, $V_{NC\_}$ with 50µA sink current to AGND				180	µA
On-Leakage Current ($I_{COM\_(ON)}$)	V_{BATT} = 5.5V, $V_{COM\_}$ = 0V or 5.5V, $V_{NO\_}$, and $V_{NC\_}$ are unconnected		-250		+250	nA
USB HIGH-SPEED SWITCH AC PERFORMANCE						
On-Channel -3dB Bandwidth (BW)	R_L = R_S = 50Ω, signal = 0dBm			950		MHz
Off-Isolation (V_{ISO})	$V_{NO\_}$, $V_{NC\_}$ = 0dBm, R_L = R_S = 50Ω, Figure 1	f = 10MHz		-48		dB
		f = 250MHz		-20		
		f = 500MHz		-17		
Crosstalk (V_{CT})	$V_{NO\_}$, $V_{NC\_}$ = 0dBm, R_L = R_S = 50Ω, Figure 1 (Note 9)	f = 10MHz		-73		dB
		f = 250MHz		-54		
		f = 500MHz		-33		
USB HIGH-SPEED SWITCH LOGIC INPUT (CB)						
Input Logic-High (V_{IH})			1.4			V
Input Logic-Low (V_{IL})					0.4	V
Input Leakage Current (I_{IN})			-250		+250	nA

µPMICs for Multimedia Application Processors in a 3.0mm x 2.5mm WLP

ELECTRICAL CHARACTERISTICS (continued)

(*Typical Operating Circuit*, V_{IN} = 3.7V, C_{BATT} = C_{IN1} = C_{IN2} = 2.2µF, C_{REFBP} = 0.1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 3, 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
USB HIGH-SPEED SWITCH DYNAMIC					
Turn-On Time (t_{ON})	$V_{NO\_}$ or $V_{NC\_}$ = 1.5V, R_L = 300Ω, C_L = 35pF, $V_{/ENUSB}$ = V_{BATT} to 0V, Figure 2		1	5	µs
Turn-Off Time (t_{OFF})	$V_{NO\_}$ or $V_{NC\_}$ = 1.5V, R_L = 300Ω, C_L = 35pF, $V_{/ENUSB}$ = 0V to V_{BATT}, Figure 2		1	5	µs
Propagation Delay (t_{PLH}, t_{PHL})	R_L = R_S = 50Ω, Figure 3		100		ps
Fault Protection Response Time (t_{FP})	$V_{COM\_}$ = 0V to 5V step, R_L = R_S = 50Ω, V_{BATT} = 3.3V, Figure 4	0.5		5.0	µs
Fault Protection Recovery Time (t_{FPR})	$V_{COM\_}$ = 5V to 0V step, R_L = R_S = 50Ω, V_{BATT} = 3.3V, Figure 4			100	µs
Output Skew Between Switches (t_{SK})	Skew between switch 1 and 2, R_L = R_S = 50Ω, Figure 3 (Note 6)		40		ps
NO_ or NC_ Off-Capacitance ($C_{NO(OFF)}$ or $C_{NC(OFF)}$)	f = 1MHz, Figure 5 (Note 6)		2		pF
COM Off-Capacitance ($C_{COM(OFF)}$)) (Note 6)	f = 1MHz, Figure 5		5.5		pF
	f = 240 MHz, Figure 5		4.8		
COM On-Capacitance ($C_{COM(ON)}$)) (Note 6)	f = 1MHz, Figure 5		6.5		pF
	f = 240 MHz, Figure 5		5.5		
Total Harmonic Distortion Plus Noise	$V_{COM\_}$ = $1V_{P-P}$, V_{BIAS} = 1V, R_L = R_S = 50Ω, f = 20Hz to 20kHz		0.03		%
USB HIGH-SPEED SWITCH—ESD PROTECTION					
$\overline{ENUSB}$, CB, NC1, NC2, NO1, NO2	Human Body Model		±2		kV
COM1, COM2	Human Body Model		±15		kV
	IEC 61000-4-2 Air-Gap Discharge		±15		
	IEC 61000-4-2 Contact Discharge		±8		
I²C SERIAL INTERFACE (Figure 8)					
Clock Frequency				400	kHz
Bus-Free Time Between START and STOP (t_{BUF})		1.3			µs
Hold Time Repeated START Condition (t_{HD_STA})		0.6			µs
SCL Low Period (t_{LOW})		1.3			µs
SCL High Period (t_{HIGH})		0.6			µs
Setup Time Repeated START Condition (t_{SU_STA})		0.6			µs
SDA Hold Time (t_{HD_DAT})		0			µs
SDA Setup time (t_{SU_DAT})		100			ns
Setup Time for STOP Condition (t_{SU_STO})		0.6			µs

ELECTRICAL CHARACTERISTICS (continued)

(*Typical Operating Circuit*, V_{IN} = 3.7V, C_{BATT} = C_{IN1} = C_{IN2} = 2.2µF, C_{REFBP} = 0.1µF, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
Maximum Pulse Width of Spikes Suppressed				50		ns
LOAD SWITCH (LS)						
Input Supply Operating Range (V_{BUCK})	After V_{BUCK} starts up		0.8		2.4	V
On-Resistance ($R_{DS(ON)}$)	V_{BUCK} = 1.0V, I_{LS} = 300mA, T_A = +25°C			50	100	mΩ
Turn-On Delay Time (t_{ON_DLY})	V_{LS} = 2.4V, R_L = 400Ω, V_{ENLS} = 1.8V, Register LSTOD = 0 (Note 6)	C_L = 0.1µF		0.85		µs
		C_L = 1µF		0.85		
		C_L = 3µF		0.85		
	V_{LS} = 2.4V, R_L = 400Ω, V_{ENLS} = 1.8V, Register LSTOD = 1	C_L = 0.1µF		30		
		C_L = 1µF		34		
		C_L = 3µF		37		
LS Rise Time (t_R)	V_{LS} = 2.4V, R_L = 400Ω, V_{ENLS} = 1.8V, Register LSRT = 0	C_L = 0.1µF		10		µs
		C_L = 1µF (Note 6)		10		
		C_L = 3µF (Note 6)		10		
	V_{LS} = 2.4V, R_L = 400Ω, V_{ENLS} = 1.8V, Register LSRT = 1	C_L = 0.1µF		25		
		C_L = 1µF		27		
		C_L = 3µF		30		
	V_{LS} = 2.4V, R_L = 400Ω, V_{ENLS} = 1.8V, Register LSRT = 2	C_L = 0.1µF		100		
		C_L = 1µF		100		
		C_L = 3µF		100		
	V_{LS} = 2.4V, R_L = 400Ω, V_{ENLS} = 1.8V, Register LSRT = 3	C_L = 0.1µF		300		
		C_L = 1µF		300		
		C_L = 3µF		300		
Turn-Off Delay Time (t_{OFF_DLY})	V_{LS} = 2.4V, R_L = 400Ω, V_{ENLS} = 1.8V	C_L = 0.1µF		11		µs
		C_L = 1µF		11		
		C_L = 3µF		11		
LS Fall Time (t_F)	V_{LS} = 2.4V, R_L = 400Ω, V_{ENLS} = 1.8V	C_L = 0.1µF		15		µs
		C_L = 1µF		150		
		C_L = 3µF		447		
Shutdown Output Resistance	V_{LS} = 2.4V, V_{ENLS} = 0V, LS_ADEN = 1			100	200	Ω

Note 3: V_{IN1}, V_{IN2}, and V_{BATT} are connected together and single input is referred to as V_{IN}.

Note 4: All units are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Note 5: When the input voltage is greater than 2.85V (typ), the UVLO comparator trips, and the threshold is reduced to 2.35V (typ). This allows the system to start normally even if the input voltage decays to 2.35V.

Note 6: Not production tested; guaranteed by design.

Note 7: $\Delta R_{ON(MAX)} = |R_{ON(CH1)} - R_{ON(CH2)}|$.

Note 8: Flatness is defined as the difference between the maximum and minimum value of on-resistance, as measured over specified analog signal ranges.

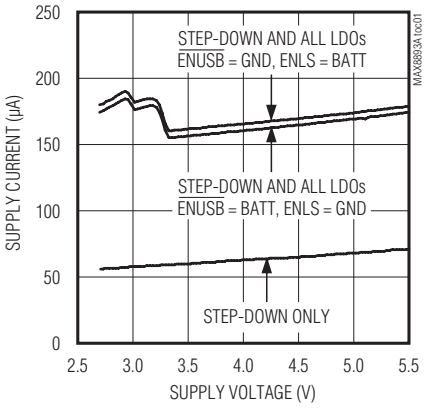
Note 9: Between any two switches.

µPMICs for Multimedia Application Processors in a 3.0mm x 2.5mm WLP

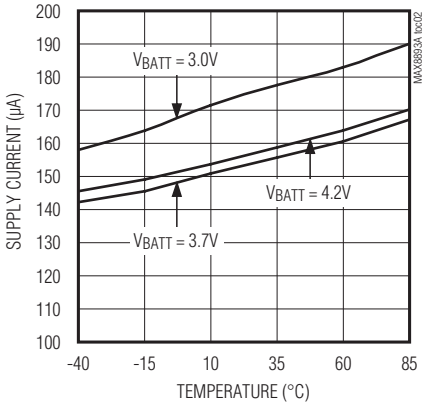
Typical Operating Characteristics

(Typical Operating Circuit, V_{IN} = 3.7V, C_{BATT} = C_{IN1} = C_{IN2} = 2.2µF, C_{REFBP} = 0.1µF, T_A = +25°C, unless otherwise noted.)

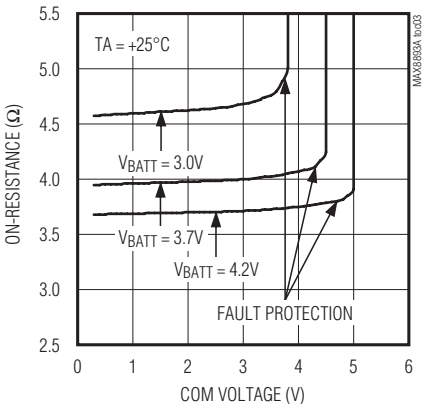
NO-LOAD SUPPLY CURRENT vs. SUPPLY VOLTAGE



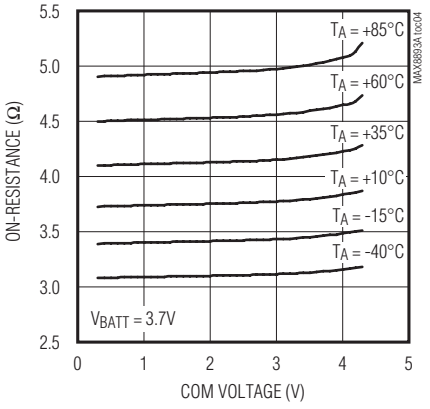
NO-LOAD SUPPLY CURRENT vs. TEMPERATURE



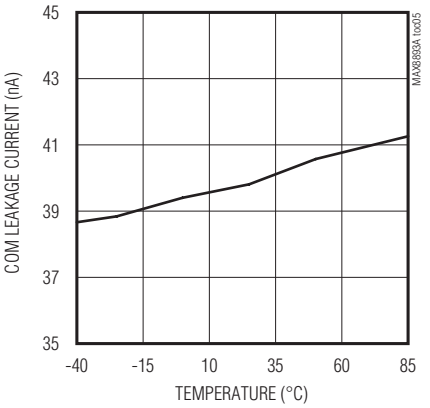
USB SWITCH ON-RESISTANCE vs. COM VOLTAGE



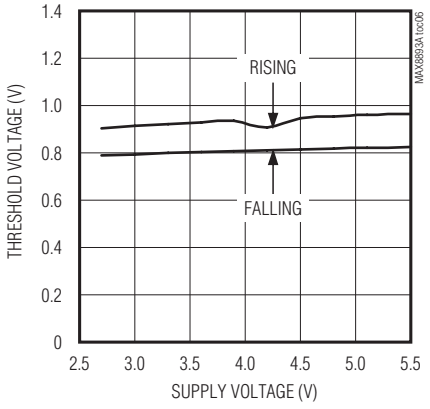
USB SWITCH ON-RESISTANCE vs. COM VOLTAGE



COM LEAKAGE CURRENT vs. TEMPERATURE



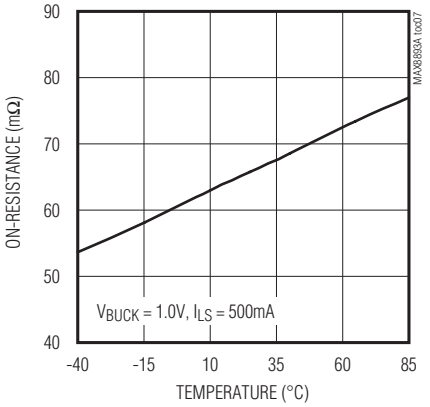
LOGIC THRESHOLD VOLTAGE vs. SUPPLY VOLTAGE



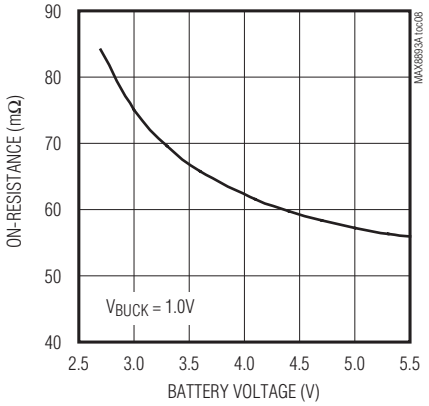
Typical Operating Characteristics (continued)

(Typical Operating Circuit, V_{IN} = 3.7V, C_{BATT} = C_{IN1} = C_{IN2} = 2.2µF, C_{REFBP} = 0.1µF, T_A = +25°C, unless otherwise noted.)

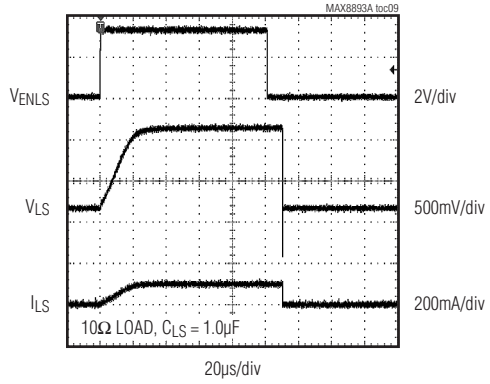
LOAD SWITCH ON-RESISTANCE vs. TEMPERATURE



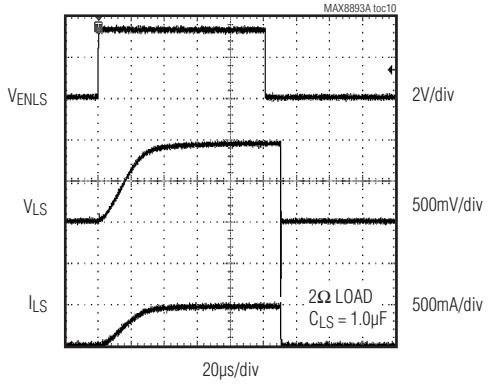
LOAD SWITCH ON-RESISTANCE vs. BATTERY VOLTAGE



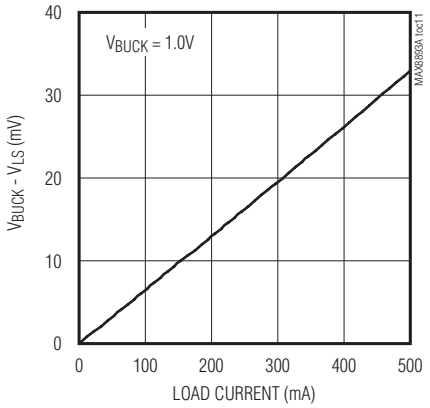
LOAD SWITCH TURN-ON/OFF WAVEFORM



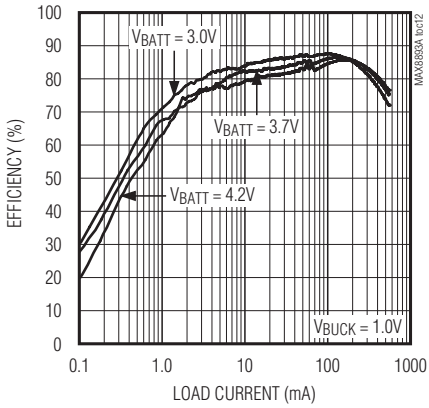
LOAD SWITCH TURN-ON/OFF WAVEFORM



LOAD SWITCH VOLTAGE DROP vs. LOAD CURRENT



STEP-DOWN EFFICIENCY vs. LOAD CURRENT

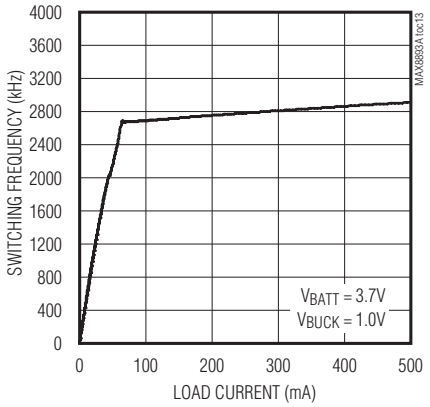


µPMICs for Multimedia Application Processors in a 3.0mm x 2.5mm WLP

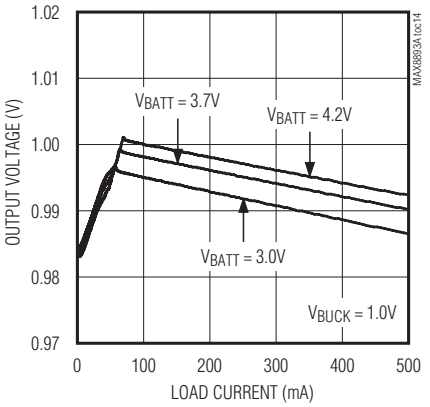
Typical Operating Characteristics (continued)

(Typical Operating Circuit, V_{IN} = 3.7V, C_{BATT} = C_{IN1} = C_{IN2} = 2.2µF, C_{REFBP} = 0.1µF, T_A = +25°C, unless otherwise noted.)

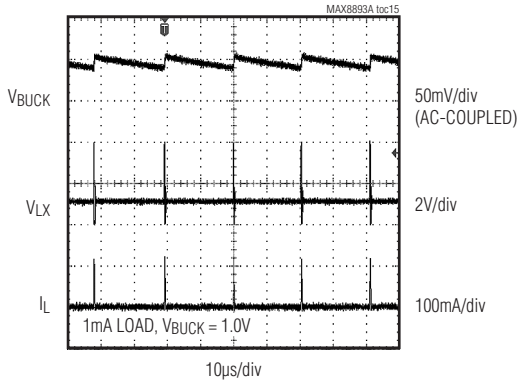
STEP-DOWN SWITCHING FREQUENCY vs. LOAD CURRENT



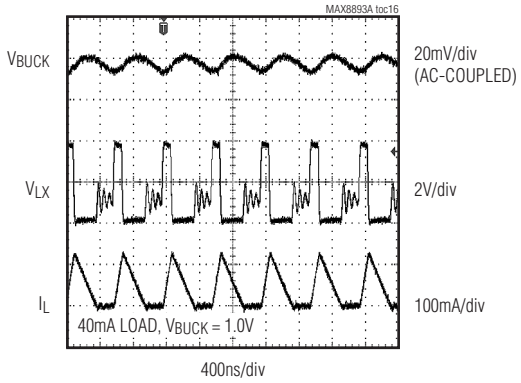
STEP-DOWN OUTPUT VOLTAGE vs. LOAD CURRENT



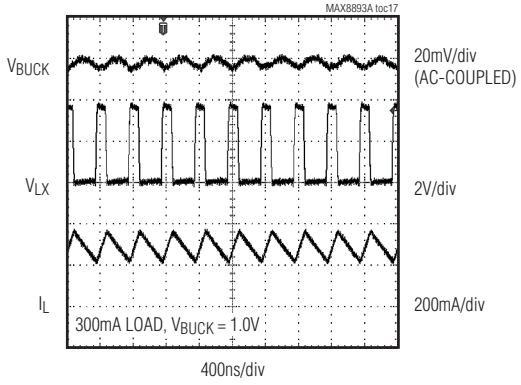
STEP-DOWN LIGHT-LOAD SWITCHING WAVEFORMS



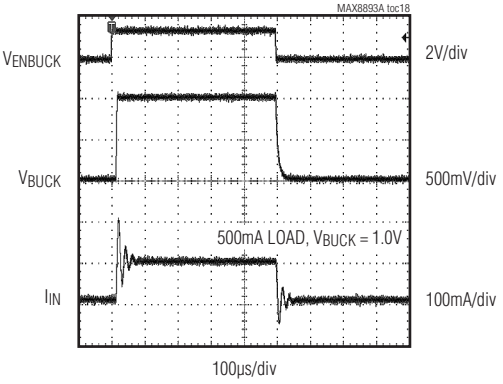
STEP-DOWN MEDIUM-LOAD SWITCHING WAVEFORMS



STEP-DOWN HEAVY-LOAD SWITCHING WAVEFORMS



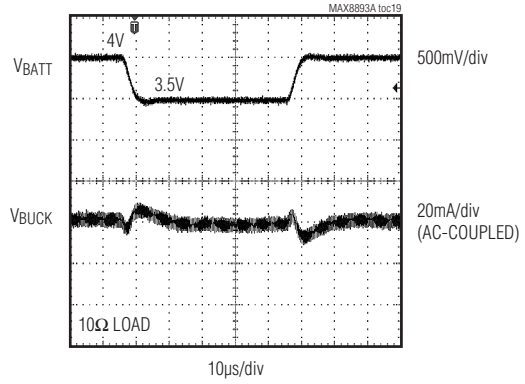
STEP-DOWN STARTUP AND SHUTDOWN WAVEFORM



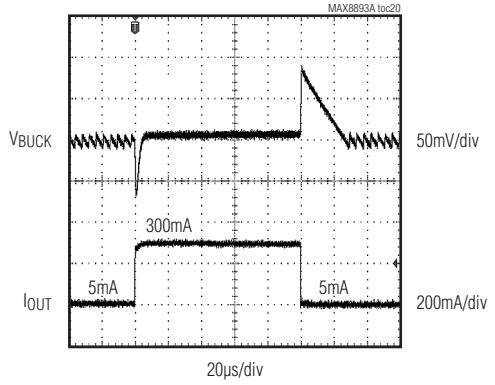
Typical Operating Characteristics (continued)

(Typical Operating Circuit, V_{IN} = 3.7V, C_{BATT} = C_{IN1} = C_{IN2} = 2.2µF, C_{REFBP} = 0.1µF, T_A = +25°C, unless otherwise noted.)

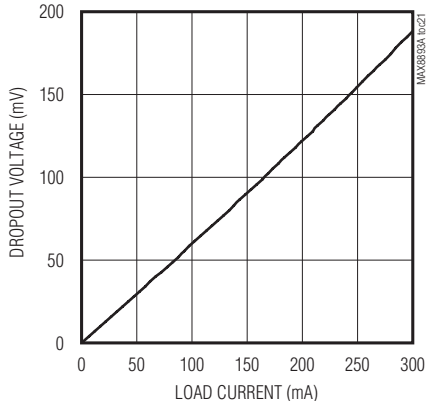
STEP-DOWN LINE TRANSIENT WAVEFORM



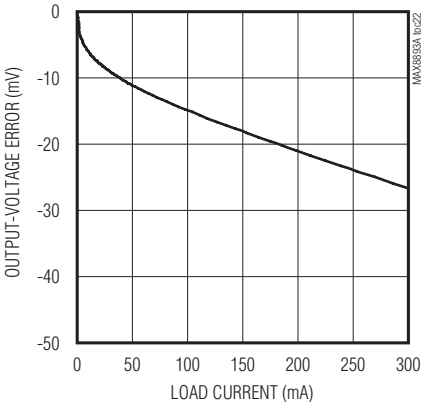
STEP-DOWN LOAD TRANSIENT WAVEFORM



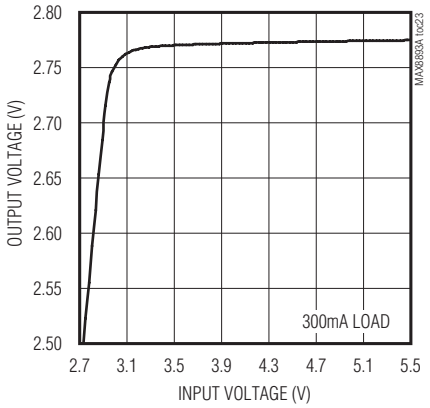
LDO1 DROPOUT VOLTAGE vs. LOAD CURRENT



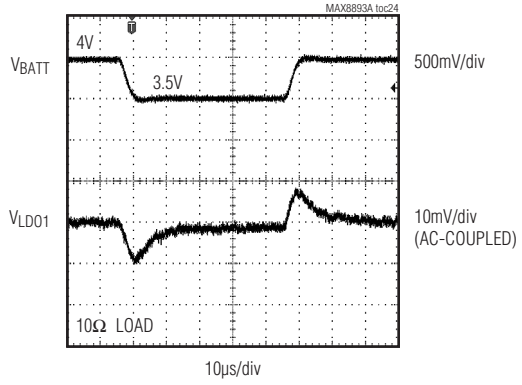
LDO1 OUTPUT-VOLTAGE ERROR vs. LOAD CURRENT



LDO1 OUTPUT VOLTAGE vs. INPUT VOLTAGE



LDO1 LINE TRANSIENT WAVEFORM

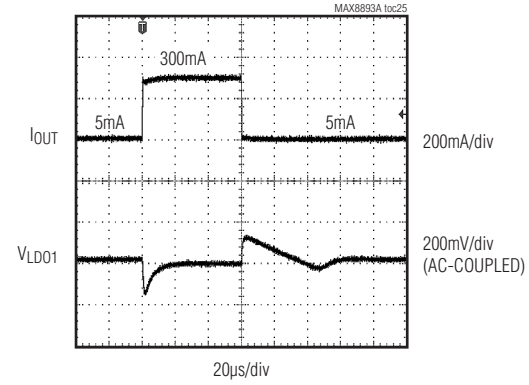


µPMICs for Multimedia Application Processors in a 3.0mm x 2.5mm WLP

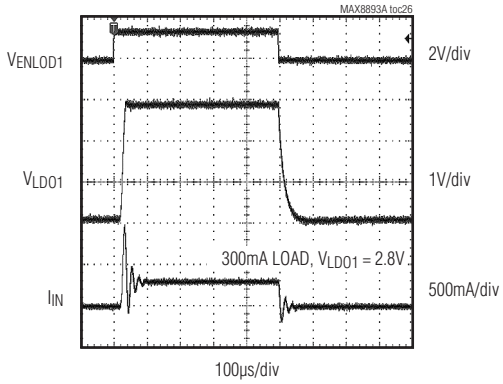
Typical Operating Characteristics (continued)

(Typical Operating Circuit, V_{IN} = 3.7V, C_{BATT} = C_{IN1} = C_{IN2} = 2.2µF, C_{REFBP} = 0.1µF, T_A = +25°C, unless otherwise noted.)

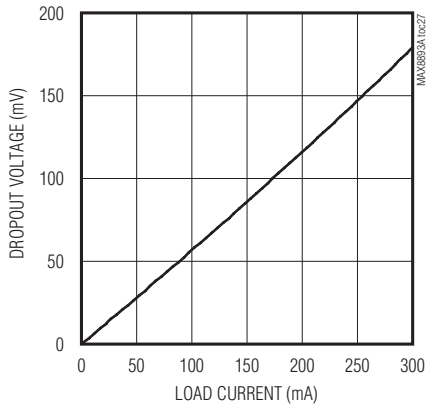
LDO1 LOAD TRANSIENT WAVEFORM



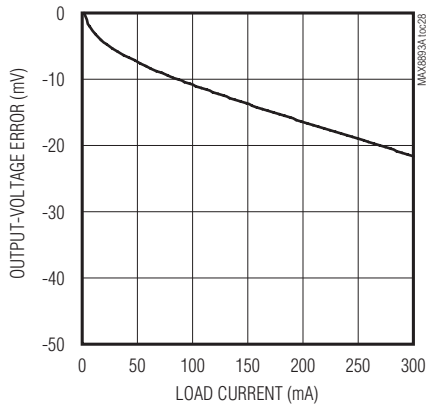
LDO1 STARTUP AND SHUTDOWN WAVEFORM



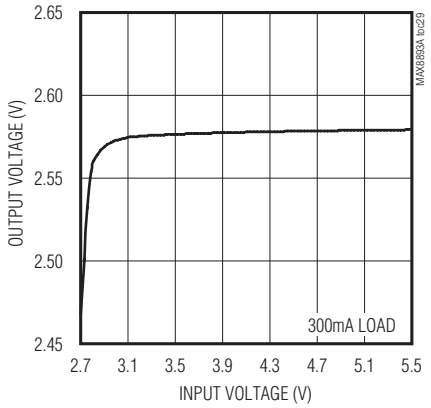
LDO2 DROPOUT VOLTAGE vs. LOAD CURRENT



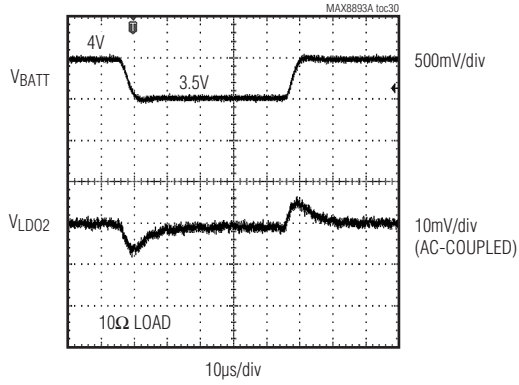
LDO2 OUTPUT-VOLTAGE ERROR vs. LOAD CURRENT



LDO2 OUTPUT VOLTAGE vs. INPUT VOLTAGE



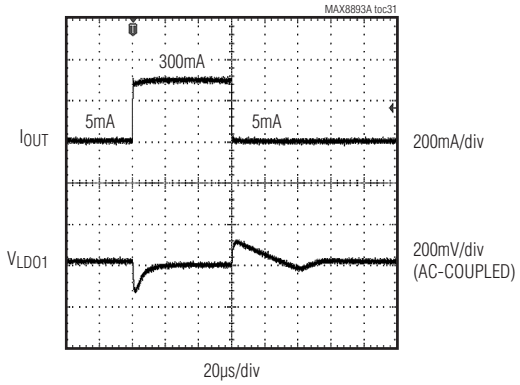
LDO2 LINE TRANSIENT WAVEFORM



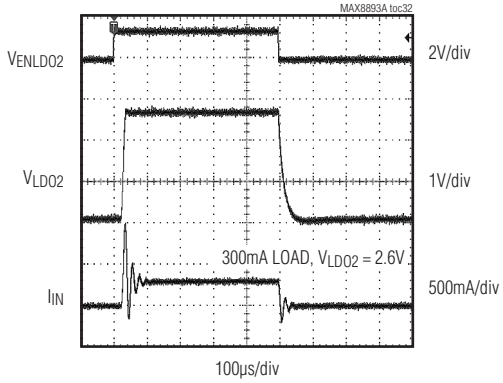
Typical Operating Characteristics (continued)

(Typical Operating Circuit, V_{IN} = 3.7V, C_{BATT} = C_{IN1} = C_{IN2} = 2.2µF, C_{REFBP} = 0.1µF, T_A = +25°C, unless otherwise noted.)

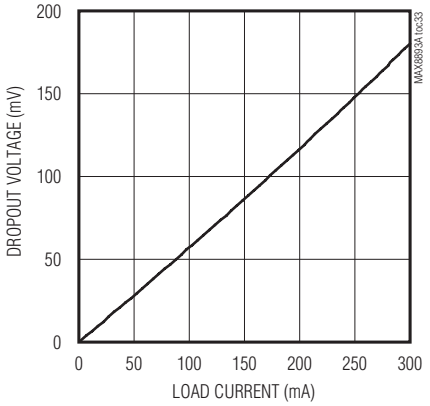
LDO2 LOAD TRANSIENT WAVEFORM



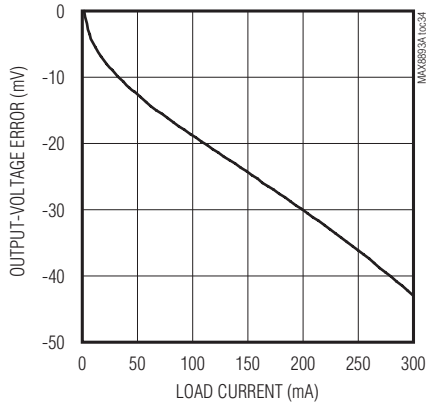
LDO2 STARTUP AND SHUTDOWN WAVEFORM



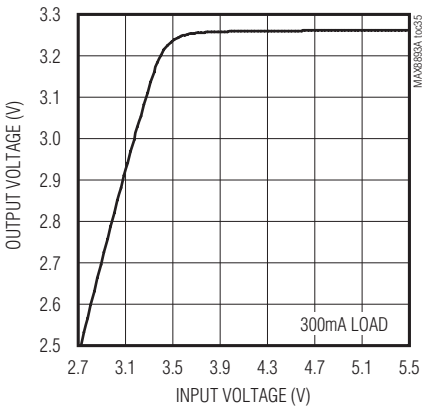
LDO3 DROPOUT VOLTAGE vs. LOAD CURRENT



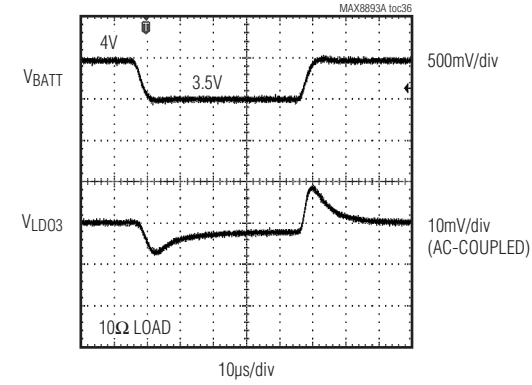
LDO3 OUTPUT-VOLTAGE ERROR vs. LOAD CURRENT



LDO3 OUTPUT VOLTAGE vs. INPUT VOLTAGE



LDO3 LINE TRANSIENT WAVEFORM

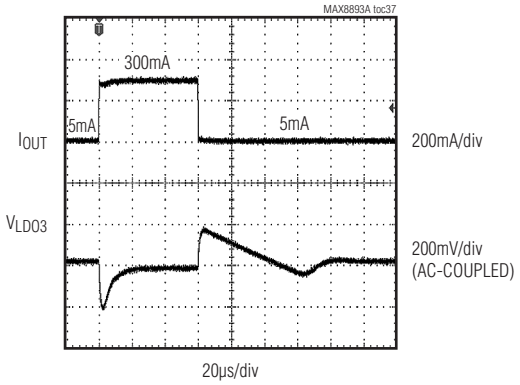


FPMIC for Multimedia Application Processor in 2.5mm x 3.0mm WLP

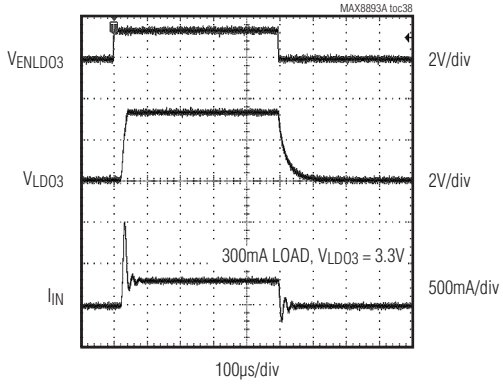
Typical Operating Characteristics (continued)

(*Typical Operating Circuit*, V_{IN} = 3.7V, C_{BATT} = C_{IN1} = C_{IN2} = 2.2µF, C_{REFBP} = 0.1µF, T_A = +25°C, unless otherwise noted.)

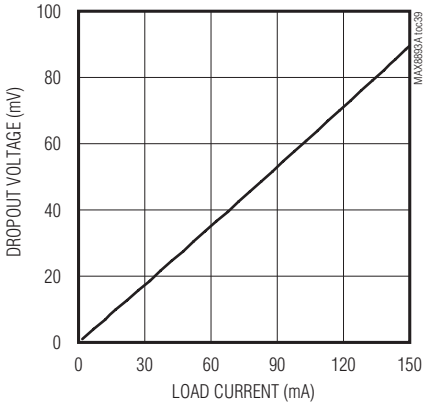
LDO3 LOAD TRANSIENT WAVEFORM



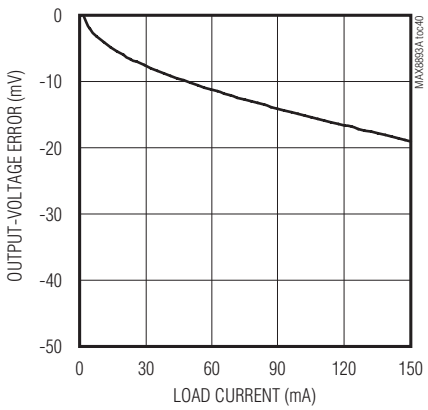
LDO3 STARTUP AND SHUTDOWN WAVEFORM



LDO4 DROPOUT VOLTAGE vs. LOAD CURRENT



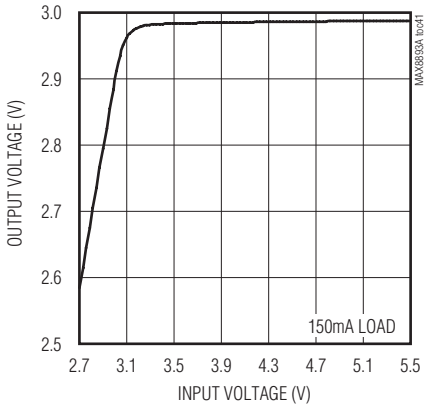
LDO4 OUTPUT-VOLTAGE ERROR vs. LOAD CURRENT



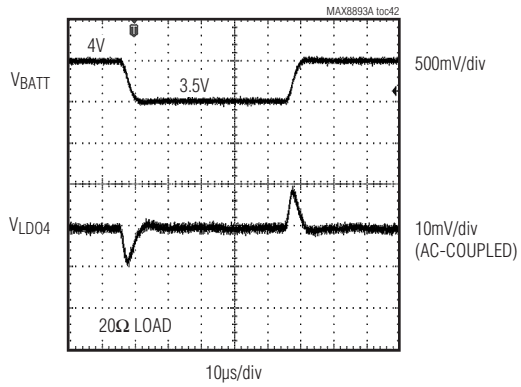
Typical Operating Characteristics (continued)

(Typical Operating Circuit, V_{IN} = 3.7V, C_{BATT} = C_{IN1} = C_{IN2} = 2.2µF, C_{REFBP} = 0.1µF, T_A = +25°C, unless otherwise noted.)

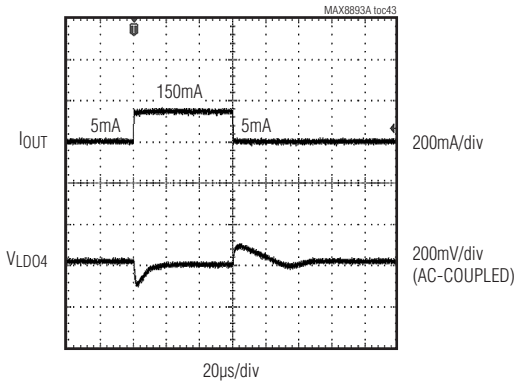
LDO4 OUTPUT VOLTAGE INPUT VOLTAGE



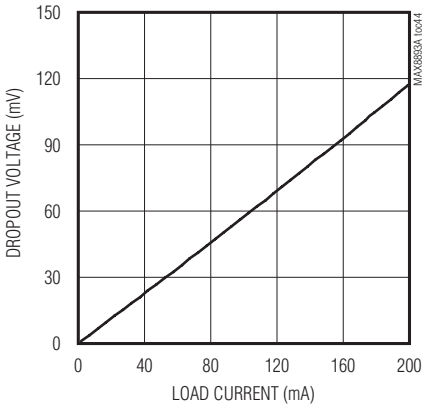
LDO4 LINE TRANSIENT WAVEFORM



LDO4 LOAD TRANSIENT WAVEFORM



LDO5 DROPOUT VOLTAGE vs. LOAD CURRENT

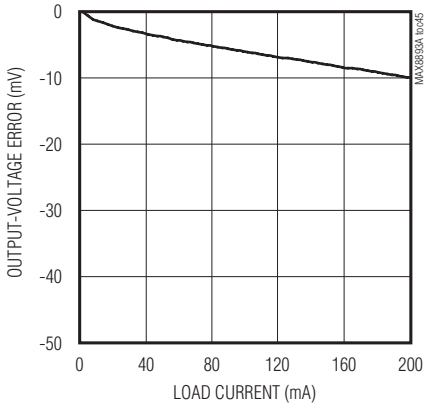


µPMICs for Multimedia Application Processors in a 3.0mm x 2.5mm WLP

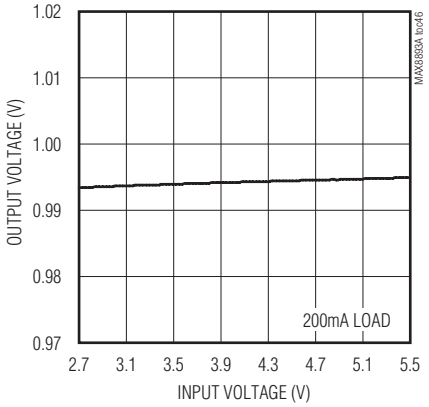
Typical Operating Characteristics (continued)

(*Typical Operating Circuit*, V_{IN} = 3.7V, C_{BATT} = C_{IN1} = C_{IN2} = 2.2µF, C_{REFBP} = 0.1µF, T_A = +25°C, unless otherwise noted.)

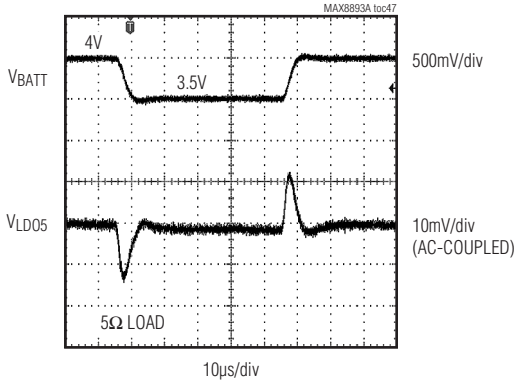
LDO4 OUTPUT-VOLTAGE ERROR vs. LOAD CURRENT



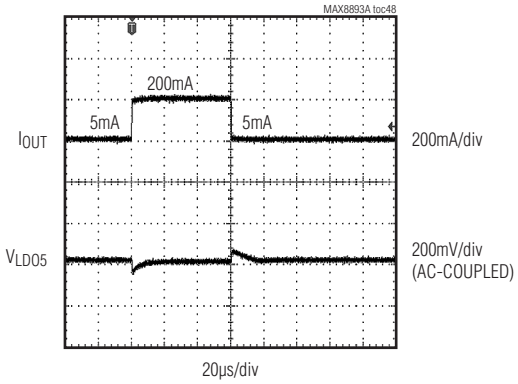
LDO5 OUTPUT VOLTAGE vs. INPUT VOLTAGE



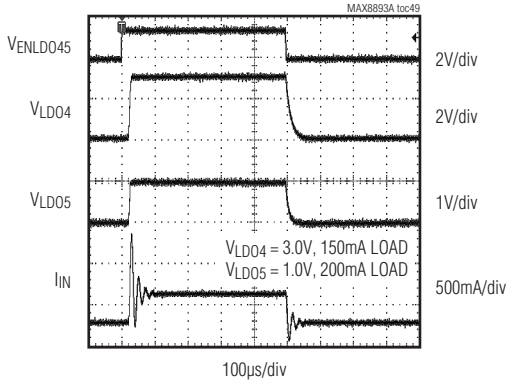
LDO5 LINE TRANSIENT WAVEFORM



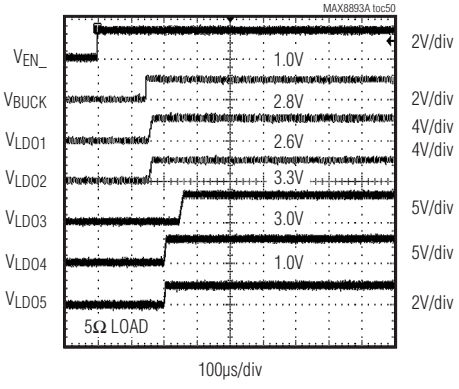
LDO5 LOAD TRANSIENT WAVEFORM



LDO4 AND LDO5 STARTUP AND SHUTDOWN WAVEFORM



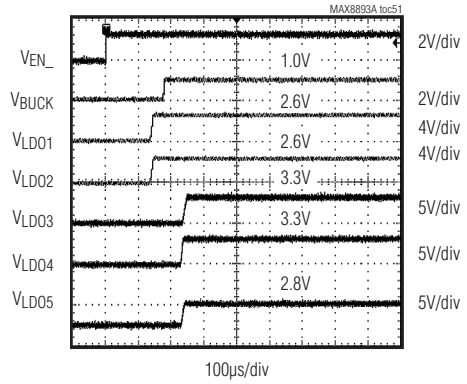
POWER-UP SEQUENCING (MAX8893A)



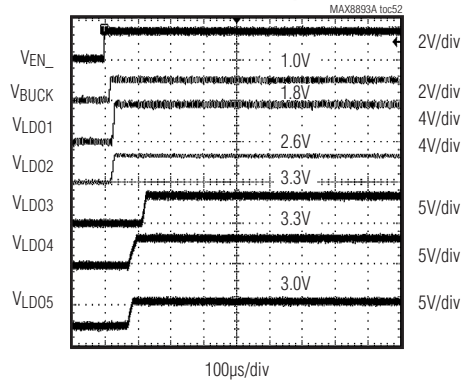
Typical Operating Characteristics (continued)

(Typical Operating Circuit, V_{IN} = 3.7V, C_{BATT} = C_{IN1} = C_{IN2} = 2.2µF, C_{REFBP} = 0.1µF, T_A = +25°C, unless otherwise noted.)

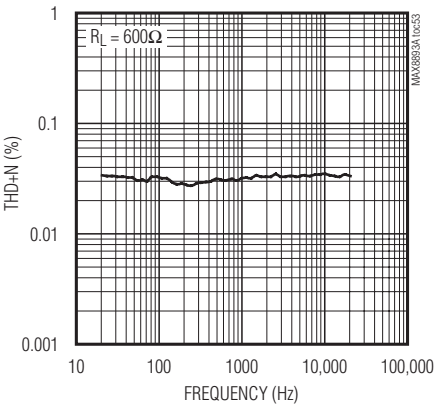
POWER-UP SEQUENCING (MAX8893B)



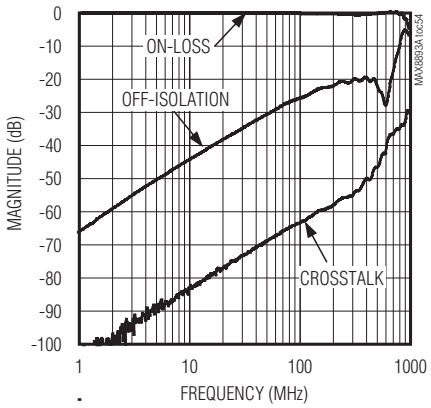
POWER-UP SEQUENCING (MAX8893C)



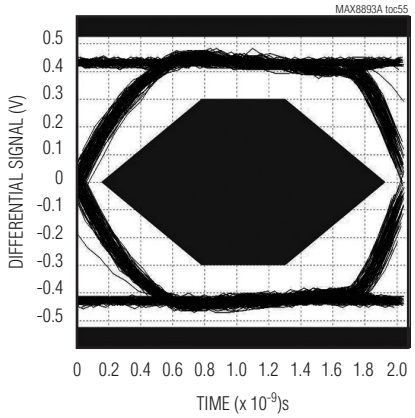
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



FREQUENCY RESPONSE



EYE DIAGRAM



µPMICs for Multimedia Application Processors in a 3.0mm x 2.5mm WLP

Test Circuits/Timing Diagrams

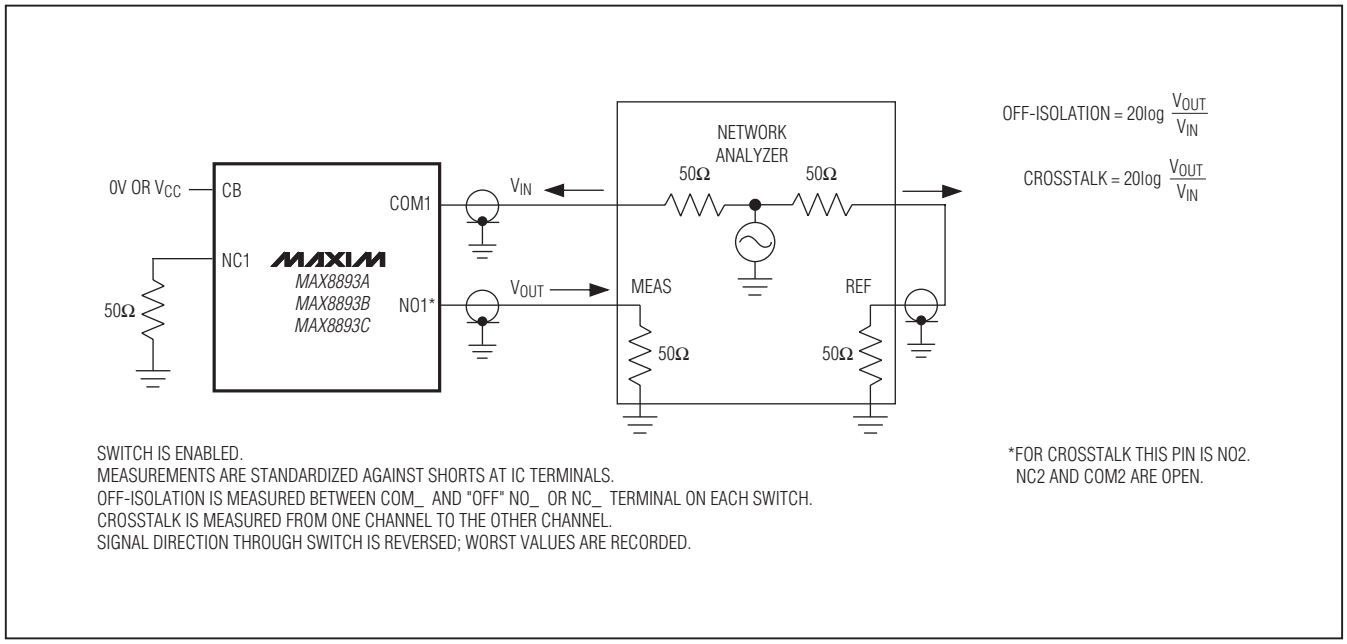


Figure 1. USB High-Speed Switch Off-Isolation and Crosstalk

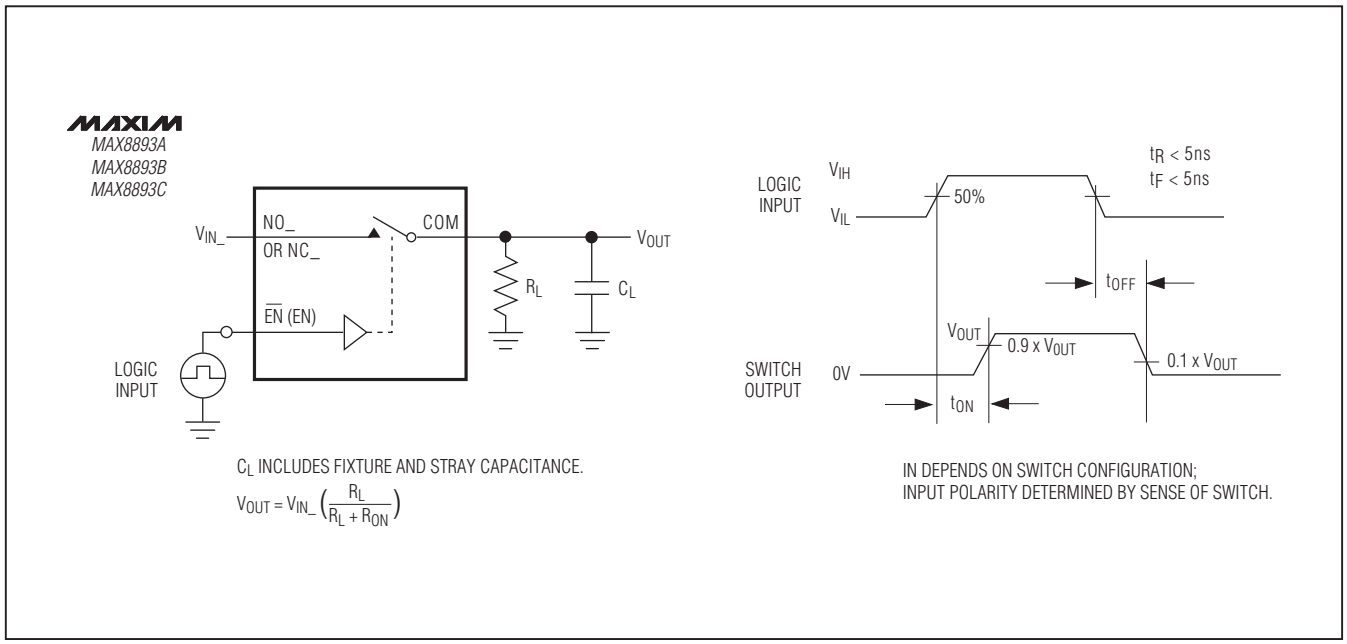


Figure 2. USB High-Speed Switch Switching Time

Test Circuits/Timing Diagrams (continued)

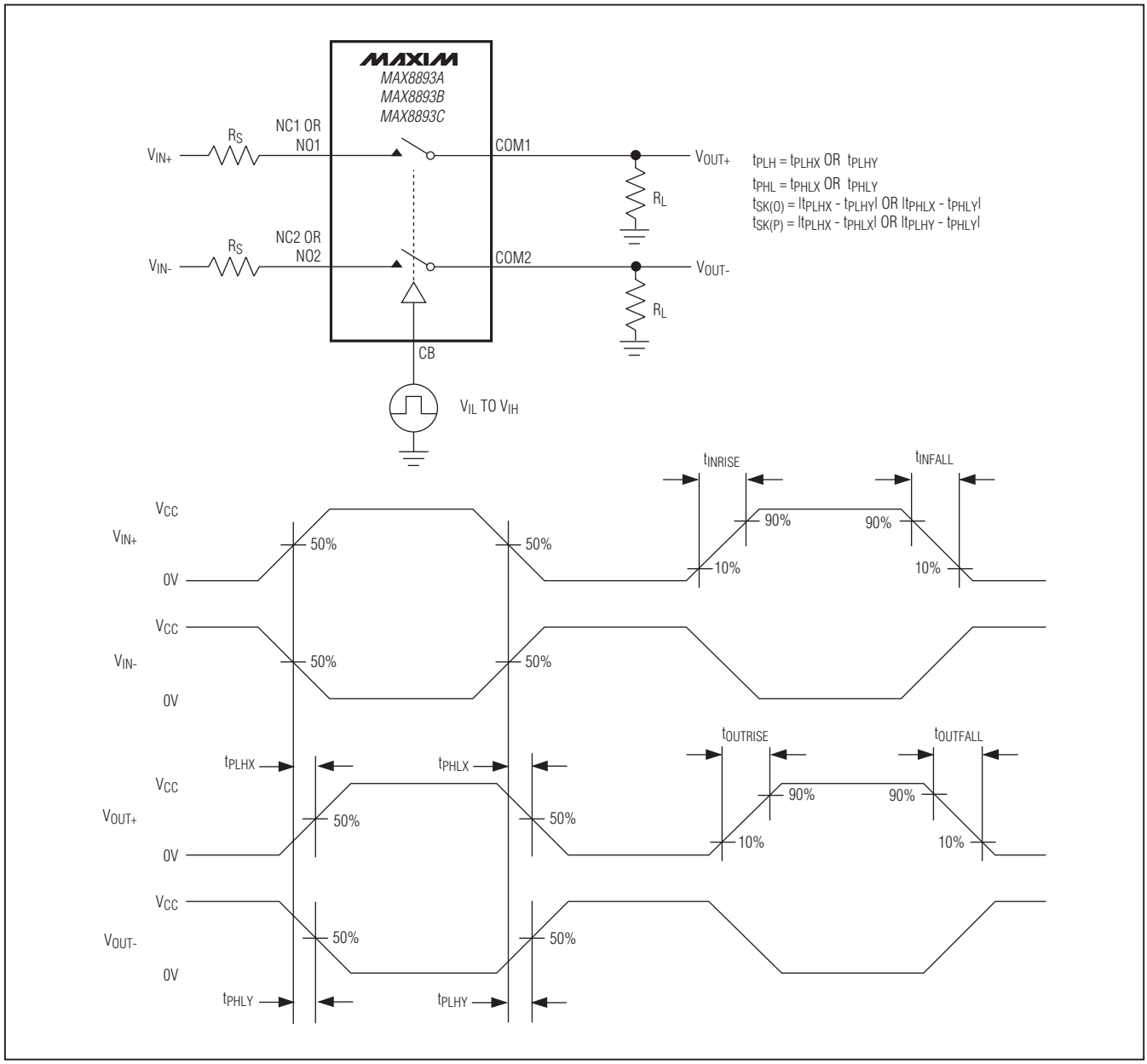


Figure 3. USB High-Speed Switch Output Signal Skew, Rise/Fall Time, Propagation Delay

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Test Circuits/Timing Diagrams (continued)

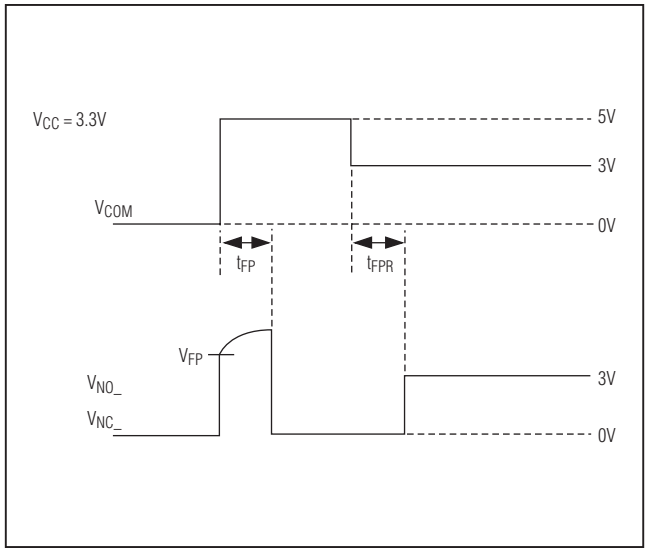


Figure 4. USB High-Speed Switch Fault-Protection Response/ Recovery Time

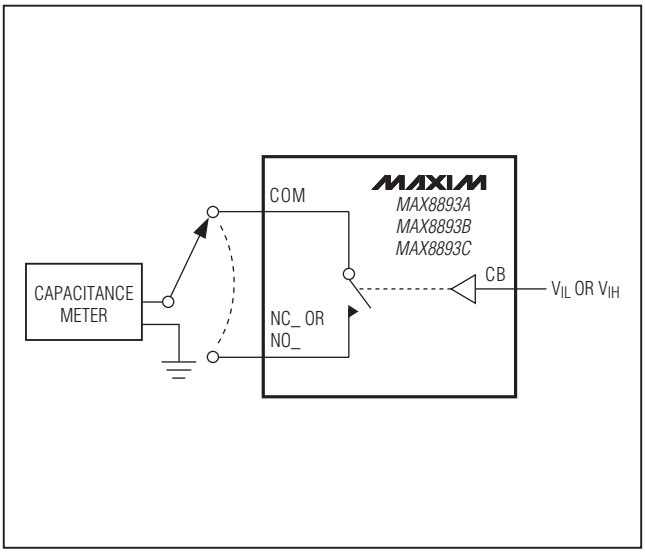
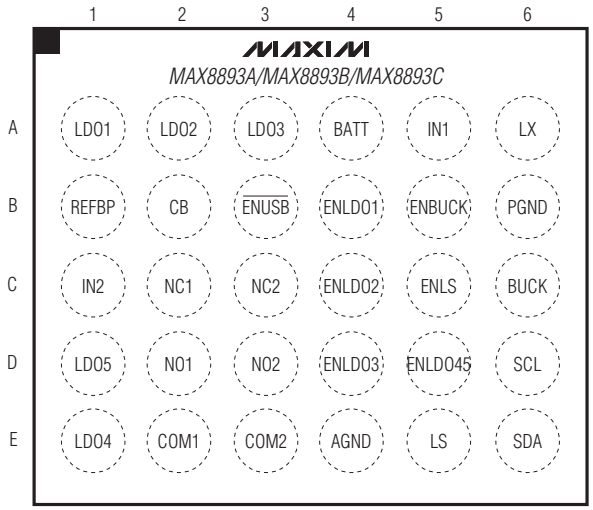


Figure 5. USB High-Speed Switch Channel Off-/On-Capacitance

Pin Configuration

TOP VIEW
(BUMPS ON BOTTIOM)



WLP
(3.0mm x 2.5mm)

Pin Description

PIN	NAME	FUNCTION
A1	LDO1	300mA LDO1 Output. Bypass LDO1 to AGND with a 2.2µF ceramic capacitor. The output voltage is programmable from 1.6V to 3.3V in 100mV steps. The output impedance of LDO1 is 300Ω when disabled with the LDO1_ADEN bit set to 1.
A2	LDO2	300mA LDO2 Output. Bypass LDO2 to AGND with a 2.2µF ceramic capacitor. The output voltage is programmable from 1.2V to 3.3V in 100mV steps. The output impedance of LDO2 is 300Ω when disabled with the LDO2_ADEN bit set to 1.
A3	LDO3	300mA LDO3 Output. Bypass LDO3 to AGND with a 2.2µF ceramic capacitor. The output voltage is programmable from 1.6V to 3.3V in 100mV steps. The output impedance of LDO3 is 300Ω when disabled with the LDO3_ADEN bit set to 1.
A4	BATT	Supply Voltage to the Control Section, LDO2, LDO3, and USB Switch. Connect a 2.2µF ceramic capacitor from BATT to AGND.
A5	IN1	Supply Voltage to the Step-Down Converter. Connect a 2.2µF input ceramic capacitor from IN1 to PGND.
A6	LX	Inductor Connection for Step-Down Converter. LX is internally connected to the drain of the internal p-channel MOSFET and the drain of the internal n-channel synchronous rectifier. The output impedance of LX is 300Ω when the step-down converter is disabled with the BUCK_ADEN bit set to 1.
B1	REFBP	Reference Noise Bypass. Bypass REFBP to AGND with a 0.1µF ceramic capacitor to reduce noise on the LDO outputs. REFBP is high impedance in shutdown.
B2	CB	Digital Control Input for USB High-Speed Switch. Drive CB low to connect COM1 to NC1 and COM2 to NC2. Drive CB high to connect COM1 to NO1 and COM2 to NO2.
B3	$\overline{\text{ENUSB}}$	Active-Low Enable Input for USB High-Speed Switch. Drive $\overline{\text{ENUSB}}$ high to put the switch in high impedance. Drive $\overline{\text{ENUSB}}$ low for normal operation.
B4	ENLDO1	Enable Input for LDO1. Drive ENLDO1 high to turn on the LDO1. Drive ENLDO1 low to turn off the LDO1. LDO1 can also be enabled/disabled through the I²C interface. ENLDO1 and I²C control bit are logically ORed. ENLDO1 has an internal 800kΩ pulldown resistor.
B5	ENBUCK	Enable Input for the Step-Down Converter. Drive ENBUCK high to turn on the step-down converter. Drive ENBUCK low to turn off the step-down converter. The step-down converter can also be enabled/disabled through the I²C interface. ENBUCK and I²C control bit are logically ORed. ENBUCK has an internal 800kΩ pulldown resistor.
B6	PGND	Power Ground for Step-Down Converter
C1	IN2	Supply Voltage to LDO1, LDO4, and LDO5. Connect a 2.2µF input ceramic capacitor from IN2 to AGND.

µPMICs for Multimedia Application Processors in a 3.0mm x 2.5mm WLP

Pin Description (continued)

PIN	NAME	FUNCTION
C2	NC1	Normally Closed Terminal for USB Switch 1. NC1 is high impedance in shutdown.
C3	NC2	Normally Closed Terminal for USB Switch 2. NC2 is high impedance in shutdown.
C4	ENLDO2	Enable Input for LDO2. Drive ENLDO2 high to turn on the LDO2. Drive ENLDO2 low to turn off the LDO2. LDO2 can also be enabled/disabled through the I²C interface. ENLDO2 and I²C control bit are logically ORed. ENLDO2 has an internal 800kΩ pulldown resistor.
C5	ENLS	Enable Input for Load Switch. Drive ENLS high to turn on the load switch. Drive ENLS low to turn off the load switch. The load switch can also be enabled/disabled through the I²C interface. ENLS and I²C control bit are logically ORed. ENLS has an internal 800kΩ pulldown resistor.
C6	BUCK	Voltage Feedback for Step-Down Converter
D1	LDO5	200mA LDO5 Output. Bypass LDO5 to AGND with a 2.2µF ceramic capacitor. The output voltage of LDO5 is programmable from 0.8V to 3.3V in 100mV steps. The output impedance of LDO5 is 300Ω when disabled with the LDO5_ADEN bit set to 1.
D2	NO1	Normally Open Terminal for USB Switch 1. NO1 is high impedance in shutdown.
D3	NO2	Normally Open Terminal for USB Switch 2. NO2 is high impedance in shutdown.
D4	ENLDO3	Enable Input for LDO3. Drive ENLDO3 high to turn on the LDO3. Drive ENLDO3 low to turn off the LDO3. LDO3 can also be enabled/disabled through the I²C interface. ENLDO3 and I²C control bit are logically ORed. ENLDO3 has an internal 800kΩ pulldown resistor.
D5	ENLDO45	Enable Input for LDO4 and LDO5. Drive ENLDO45 high to turn on the LDO4 and LDO5. Drive ENLDO45 low to turn off the LDO4 and LDO5. LDO4 and LDO5 can also be enabled/disabled individually through the I²C interface. ENLDO45 and I²C control bits (ELDO4 and ELDO5) are logically ORed. ENLDO45 has an internal 800kΩ pulldown resistor.
D6	SCL	I²C-Compatible Serial Interface Clock High-Impedance Input
E1	LDO4	150mA LDO4 Output. Bypass LDO4 to GND with a 1µF ceramic capacitor. The output voltage of LDO4 is programmable from 0.8V to 3.3V in 100mV steps. The output impedance of LDO4 is 300Ω when disabled with the LDO4_ADEN bit set to 1.
E2	COM1	Common Terminal for USB High Switch 1
E3	COM2	Common Terminal for USB High Switch 2
E4	AGND	Analog Ground. Ground for all the LDOs, control section, and USB switches.
E5	LS	Load Switch Output. LS is connected to the drain of an internal p-channel MOSFET. $V_{LS} = V_{BUCK} - R_{DS(ON)}$ (p-channel MOSFET) x load current.
E6	SDA	I²C-Compatible Serial Interface Data High-Impedance Input

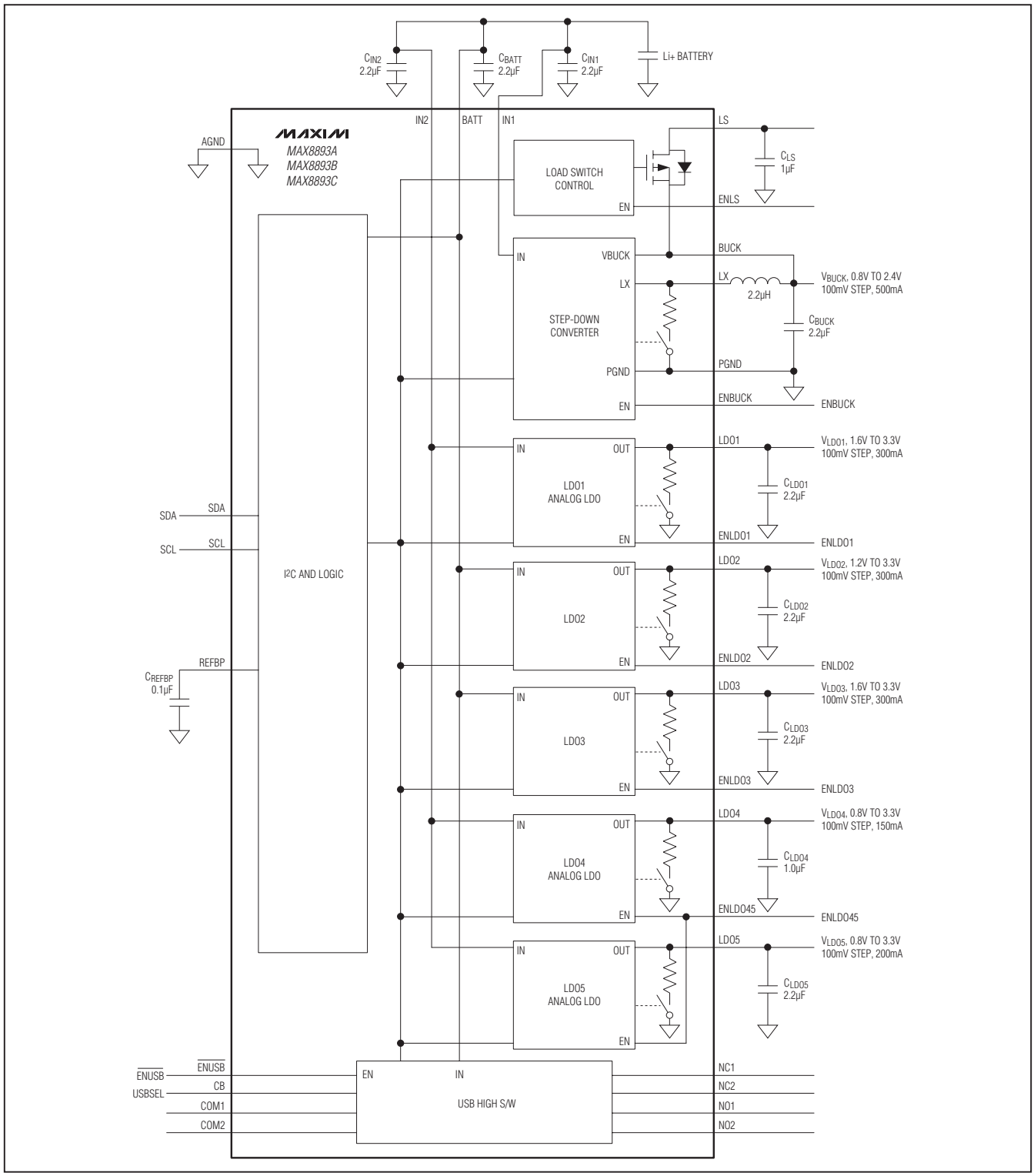


Figure 6. Block Diagram and Application Circuit

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Detailed Description

The MAX8893A/MAX8893B/MAX8893C highly integrated power-management ICs integrate a high-efficiency 500mA step-down DC-DC converter, five low-dropout linear regulators, a load switch with ultra-low on-resistance, a USB high-speed switch, and a 400kHz I²C serial interface.

The step-down converter delivers over 500mA at I²C programmable output levels from 0.8V to 2.4V. It uses a proprietary hysteretic-PWM control scheme that switches up to 4MHz, allowing a trade-off between efficiency and tiny external components. The step-down converter also features dynamic voltage scaling (DVS) control. Its output voltage ramps up with the I²C-controlled ramp rate from 1mV/µs to 12mV/µs.

Five low-dropout linear regulators feature low 45µV_{RMS} output noise (LDO1, LDO4, and LDO5) and very low ground currents (LDO2 and LDO3).

The USB high-speed switch is a high ESD-protected DPDT analog switch. It is ideal for USB 2.0 Hi-Speed (480Mbps) switching applications and also meets USB low- and full-speed requirements. The load switch features ultra-low on-resistance and operates from 0.8V to 2.4V input range. Its rise time is I²C programmable to control the inrush current. The internal I²C interface provides flexible control on regulator ON/OFF control, output voltage setting, step-down dynamic voltage scaling and ramp rate, and load switch timing.

Step-Down DC-DC Converter Control Scheme

The MAX8893A/MAX8893B/MAX8893C step-down converter is optimized for high-efficiency voltage conversion over a wide load range, while maintaining excellent transient response, minimizing external component size, and output voltage ripple. The step-down converter also features an optimized on-resistance internal MOSFET switch and synchronous rectifier to maximize efficiency. The IC utilizes a proprietary hysteretic-PWM control scheme that switches with nearly fixed frequency up to 4MHz allowing for ultra-small external components. Its output current is guaranteed up to 500mA.

When the step-down output voltage falls below the regulation threshold, the error comparator begins a switching cycle by turning on the high-side switch. This switch remains on until the minimum on-time (t_{ON}) expires and the output voltage is in regulation or the current-limit threshold is exceeded. Once off, the high-side switch remains off until the minimum off-time (t_{OFF}) expires and the output voltage again falls below the regulation threshold. During the off period, the low-side synchronous rectifier turns on and remains on until either the high-side switch turns on again or the inductor current reduces to the rectifier-off current threshold (I_{LXOFF} = 30mA (typ)). The internal synchronous rectifier eliminates the need for an external Schottky diode.

The step-down converter has the internal soft-start circuitry with a fixed ramp to eliminate input current spikes when it is enabled.

Voltage Positioning Load Regulation

The step-down converter uses a unique feedback network. By taking feedback from the LX node, the usual phase lag due to the output capacitor is removed, making the loop exceedingly stable and allowing the use of very small ceramic output capacitors. This configuration causes the output voltage to shift by the inductor series resistance multiplied by the load current. This voltage-positioning load regulation greatly reduces overshoot during load transients, which effectively halves the peak-to-peak output-voltage excursions compared to traditional step-down converters.

Dynamic Voltage Scaling (DVS) Control with Ramp Rate

The step-down output voltage has a variable ramp rate that is set by the BUCKRAMP bits in the DVS RAMP CONTROL register. This register controls the output-voltage ramp rate during a positive voltage change (for example, from 1.0V to 1.1V), and a negative voltage change (for example, from 1.1V to 1.0V). Ramp rate adjustment range is from 1mV/µs to 12mV/µs in the step of 1mV/µs.

After the step-down converter is in regulation, its output voltage can dynamically ramp up at the rate set by the BUCKRAMP bits for a positive voltage change. For a negative voltage change, the decay rate of the output voltage depends on the size of the external load: a small load results in an output-voltage decay that is slower than the specified ramp rate and LX sinks current from the output capacitor to actively ramp down the output voltage; a large load (greater than COUT x Ramp Rate) results in an output-voltage decay with the specified ramp rate.

When the step-down converter is disabled, the output voltage decays to ground at a rate determined by the output capacitance, internal discharge resistance, and the external load.

Low-Dropout Linear Regulators

The MAX8893A/MAX8893B/MAX8893C contain five low-dropout, low-quiescent-current, high-accuracy, linear regulators (LDOs). The LDO output voltages are set through the I²C serial interface. The LDOs include an internal reference, error amplifier, p-channel pass transistor, and internal programmable voltage-divider. Each error amplifier compares the reference voltage to a feedback voltage and amplifies the difference. If the feedback voltage is lower than the reference voltage, the pass-transistor gate is pulled lower, allowing more current to pass to the output and increasing the output voltage. If the feedback voltage is too high, the pass-transistor gate is pulled up, allowing less current to pass to the output.

Default Regulator Output Voltages

The default regulator output voltages are set as shown in Table 1. All regulator output voltages (BUCK, LDO1, LDO2, LDO3, LDO4, and LDO5) are programmable through the I²C serial interface.

Enable Inputs (ENBUCK, $\overline{\text{ENLDO\_}}$, ENLS, $\overline{\text{ENUSB}}$)

The MAX8893A/MAX8893B/MAX8893C have individual enable inputs for each regulator, load switch, and USB switch. The individual enable inputs (ENBUCK, ENLDO1, ENLDO2, ENLDO3, ENLDO45, ENLS) are logically ORed with the corresponding I²C serial interface control bit. $\overline{\text{ENUSB}}$ input is logically NANDed with the $\overline{\text{EUSB}}$ bit. See Tables 2, 3, and 4 for enable logic truth tables. The enable inputs (ENBUCK, ENLDO_, and ENLS) are internally pulled to AGND by an 800kΩ (typ) pulldown resistor. $\overline{\text{ENUSB}}$ is internally pulled up to BATT by an 800kΩ (typ) pullup resistor.

Any valid enable input signal turns on the MAX8893A/MAX8893B/MAX8893C. After the IC is up, the I²C interface is active and the IC can be reprogrammed through the I²C interface. To turn off the IC, both I²C bus and enable inputs must be low.

All I²C register values return to the default value when no enable input signals are present.

Table 1. Default Regulator Output Voltages

PART	BUCK (V)	LDO1 (V)	LDO2 (V)	LDO3 (V)	LDO4 (V)	LDO5 (V)
MAX8893A	1.0	2.8	2.6	3.3	3.0	1.0
MAX8893B	1.0	2.6	2.6	3.3	3.3	2.8
MAX8893C	1.0	1.8	2.6	3.3	3.3	3.0

Table 2. Truth Table for BUCK, LDO1 to LDO3, and Load Switch

ENABLE INPUT (ENBUCK, ENLDO1, ENLDO2, ENLDO3, OR ENLS)	CORRESPONDING I²C ON/OFF CONTROL BIT	CORRESPONDING REGULATOR OR SWITCH
0	0	Off
0	1	On
1	0	On
1	1	On

Table 3. Truth Table for LDO4 and LDO5

ENABLE INPUT (ENLDO45)	ELDO4 BIT	ELDO5 BIT	LDO4	LDO5
0	0	0	Off	Off
0	0	1	Off	On
0	1	0	On	Off
0	1	1	On	On
1	0	0	On	On
1	1	1	On	On

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Table 4. Truth Table for USB Switch

$\overline{ENUSB}$	$\overline{EUSB}$ BIT	USB SWITCH
0	0	On
0	1	On
1	0	On
1	1	Off

Power-Up Sequencing

Drive ENBUCK or ENLDO_ high to turn on the BUCK converter or the corresponding LDOs. When ENBUCK and ENLDO_ are connected together and driven from low to high, all the regulators are turned on with the preset power-up sequencing. There are time delays between each regulator to limit input current rush. The MAX8893A/MAX8893B/MAX8893C have different power-up time delays between each regulator. See the *Typical Operating Characteristics* for details.

Undervoltage Lockout

When V_{IN} rises above the undervoltage lockout threshold (2.85V typ), the MAX8893A/MAX8893B/MAX8893C can be enabled by driving any EN_ high or $\overline{ENUSB}$ low. The UVLO threshold hysteresis is typically 0.5V. Therefore, if V_{IN} falls below 2.35V (typ), the undervoltage lockout circuitry disables all outputs and all internal registers are reset to default values.

Reference Noise Bypass (REFBP)

Bypass REFBP to AGND with a 0.1µF ceramic capacitor to reduce noise on the LDO outputs. REFBP is high impedance in shutdown.

Thermal-Overload Protection

Thermal-overload protection limits total power dissipation in the MAX8893A/MAX8893B/MAX8893C. The step-down converter and LDOs have independent thermal protection circuits. When the junction temperature exceeds +160°C, the LDO, or step-down thermal-overload protection circuitry disables the corresponding regulators, allowing the IC to cool. The LDO thermal-overload protection circuit enables the LDOs after the LDO junction temperature cools down, resulting in pulsed LDO outputs during continuous thermal-overload conditions. The step-down converter's thermal-overload protection circuitry enables the step-down converter after the junction temperature cools down. Thermal-overload protection safeguards the IC in the event of fault conditions.

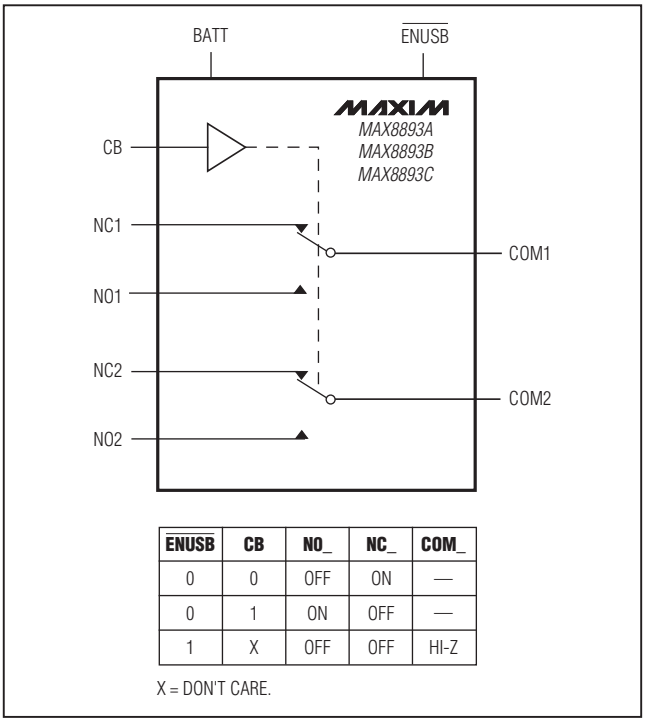
USB High-Speed Switch

The USB high-speed switch is a ±15kV ESD-protected DPDT analog switch. It is ideal for USB 2.0 Hi-Speed (480Mbps) switching applications and also meets USB low- and full-speed requirements.

The USB switch is fully specified to operate from a single 2.7V to 5.5V supply. The switch is based on charge-pump-assisted n-channel architecture. The switch also features a shutdown mode to reduce the quiescent current.

Digital Control Input

The USB high-speed switch provides a single-bit control logic input, CB. CB controls the position of the switches as shown in Figure 7. Driving CB rail-to-rail minimizes power consumption.



$\overline{ENUSB}$	CB	NO_	NC_	COM_
0	0	OFF	ON	—
0	1	ON	OFF	—
1	X	OFF	OFF	HI-Z

X = DON'T CARE.

Figure 7. USB Switch Functional Diagram/Truth Table

Analog Signal Levels

The on-resistance of the USB switch is very low and stable as the analog input signals are swept from ground to V_{IN} (see the *Typical Operating Characteristics*). These switches are bidirectional, allowing NO_, NC_, and COM_ to be configured as either inputs or outputs. The charge-pump-assisted n-channel architecture allows the switch to pass analog signals that exceed V_{IN} up to the overvoltage fault protection threshold. This allows USB signals that exceed V_{IN} to pass, allowing compliance with USB requirements for voltage levels.

Overvoltage Fault Protection

The USB switch features overvoltage fault protection on COM_. Fault protection protects the switch and USB transceiver from damaging voltage levels. When voltages on COM_ exceed the fault protection threshold (V_{FP}), COM_, NC_, and NO_ are high impedance.

Enable Input ($\overline{ENUSB}$)

The USB switch features a shutdown mode that reduces the quiescent current supply and places COM_ in high impedance. Drive $\overline{ENUSB}$ high to place the USB switch in shutdown mode. Drive $\overline{ENUSB}$ low to allow the USB switch to enter normal operation.

Load Switch

The MAX8893A/MAX8893B/MAX8893C include an ultra-low R_{ON} p-channel MOSFET load switch. The switch has its own enable input, ENLS. When it is enabled, its output soft-starts with I²C programmed rising time to avoid inrush current. See Table 8. The switch input is from the step-down converter output and can operate over the 0.8V to 2.4V range. With LS_ADEN bit set to 1, when the switch is disabled, an internal 100Ω resistor is connected between the load switch output and ground for quick discharging.

I²C Serial Interface

An I²C-compatible, 2-wire serial interface controls all the regulator output voltages, load switch timing, individual enable/disable control, and other parameters. The serial bus consists of a bidirectional serial-data line (SDA) and a serial-clock input (SCL). The MAX8893A/MAX8893B/MAX8893C are slave-only devices, relying upon a master to generate a clock signal. The master initiates data transfer to and from the MAX8893A/MAX8893B/MAX8893C and generates SCL to synchronize the data transfer (Figure 8).

I²C is an open-drain bus. Both SDA and SCL are bidirectional lines, connected to a positive supply voltage through a pullup resistor. They both have Schmitt triggers and filter circuits to suppress noise spikes on the bus to assure proper device operation.

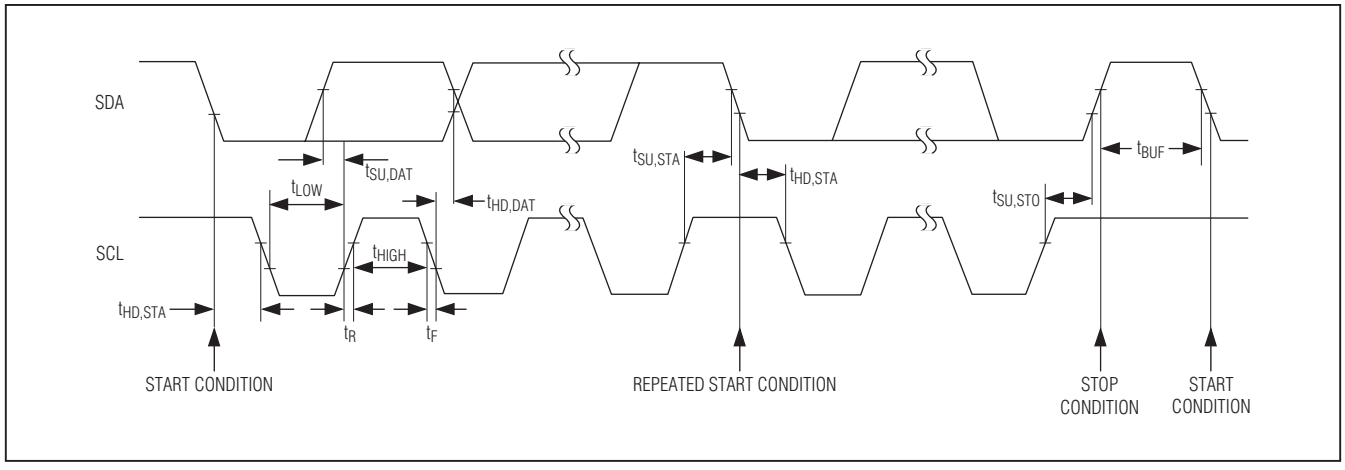


Figure 8. 2-Wire Serial Interface Timing Detail

Slave Address

A bus master initiates communication with a slave device (MAX8893A/MAX8893B/MAX8893C) by issuing a START condition followed by the slave address. The slave address byte consists of 7 address bits (0111110) and a read/write bit (RW). Its address is 0x7C for write operations and 0x7D for read operations. After receiving the proper address, the MAX8893A/MAX8893B/MAX8893C issue an acknowledge by pulling SDA low during the ninth clock cycle.

Bit Transfer

Each data bit, from the most significant bit to the least significant bit, is transferred one by one during each clock cycle. During data transfer, the SDA signal is allowed to change only during the low period of the SCL clock and it must remain stable during the high period of the SCL clock (Figure 9).

START and STOP Conditions

Both SCL and SDA remain high when the bus is not busy. The master signals the beginning of a transmission with a START (S) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the MAX8893A/MAX8893B/MAX8893C, it issues a STOP (P) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission (Figure 10). Both START and STOP conditions are generated by the bus master.

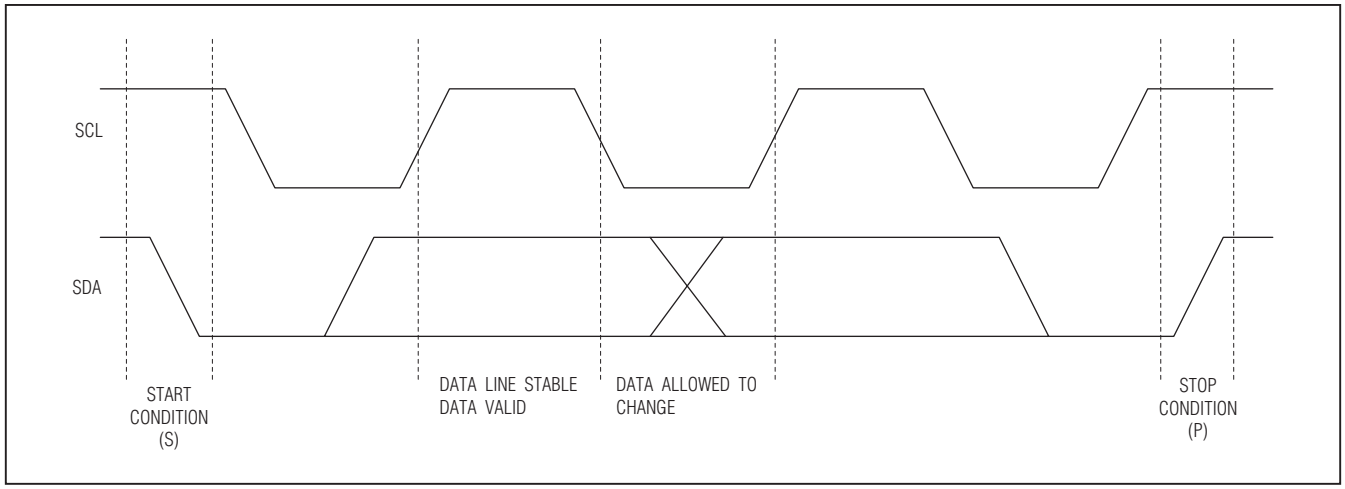


Figure 9. Bit Transfer

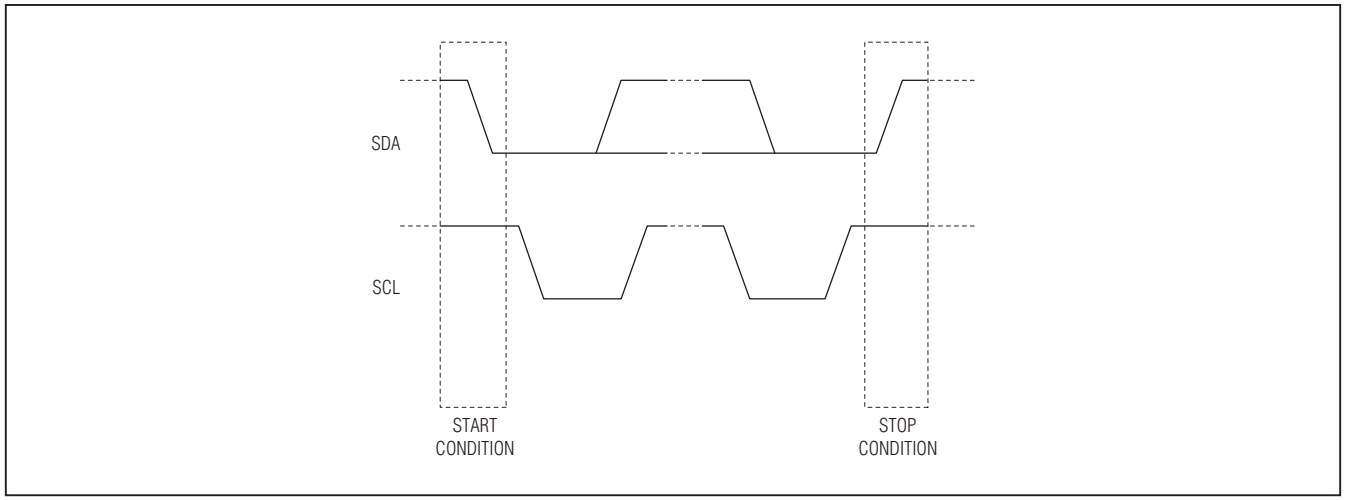


Figure 10. START and STOP Conditions

Acknowledge

The acknowledge bit is used by the recipient to handshake the receipt of each byte of data (Figure 11). After data transfer, the master generates the acknowledge clock pulse and the recipient pulls down the SDA line during this acknowledge clock pulse, such that the SDA line stays low during the high duration of the clock pulse. When the master transmits the data to the MAX8893A/MAX8893B/MAX8893C, it releases the SDA line and the MAX8893A/MAX8893B/MAX8893C take the control of the SDA line and generate the acknowledge bit. When SDA remains high during this 9th clock pulse, this is defined as the not acknowledge signal. The master can then generate either a STOP condition to abort the transfer, or a REPEATED START condition to start a new transfer.

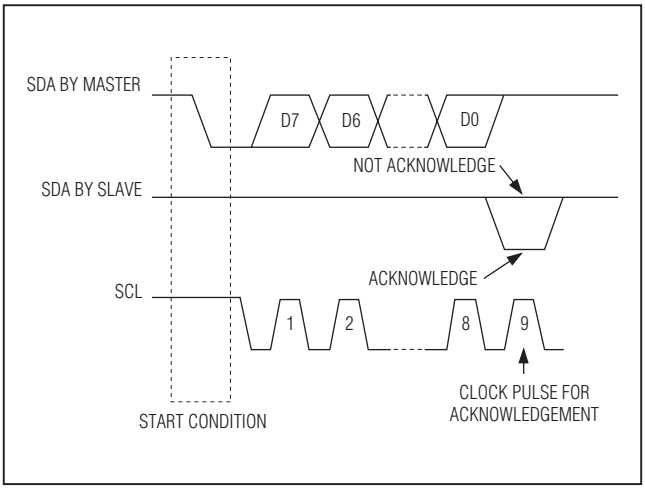


Figure 11. Acknowledge

Write Operation

The MAX8893A/MAX8893B/MAX8893C recognize the write-byte protocol as defined in the SMBus™ specification and shown in section A of Figure 12. The write-byte protocol allows the I²C master device to send 1 byte of data to the slave device. The write-byte protocol requires a register pointer address for the subsequent write. The MAX8893A/MAX8893B/MAX8893C acknowledge any register pointer even though only a subset of those registers actually exists in the device. The write-byte protocol is as follows:

1) The master sends a start command.
2) The master sends the 7-bit slave address followed by a write bit (0x7C).
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave updates with the new data.
8) The slave acknowledges the data byte.
9) The master sends a STOP condition.

In addition to the write-byte protocol, the MAX8893A/MAX8893B/MAX8893C can write to multiple registers as shown in section B of Figure 12. This protocol allows the I²C master device to address the slave only once and then send data to a sequential block of registers starting at the specified register pointer.

Use the following procedure to write to a sequential block of registers:

1) The master sends a start command.
2) The master sends the 7-bit slave address followed by a write bit (0x7C).
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends the 8-bit register pointer of the first register to write.
5) The slave acknowledges the register pointer.
6) The master sends a data byte.
7) The slave updates with the new data.
8) The slave acknowledges the data byte.
9) Steps 6 to 8 are repeated for as many registers in the block, with the register pointer automatically incremented each time.
10) The master sends a STOP condition.

SMBus is a trademark of Intel Corp.

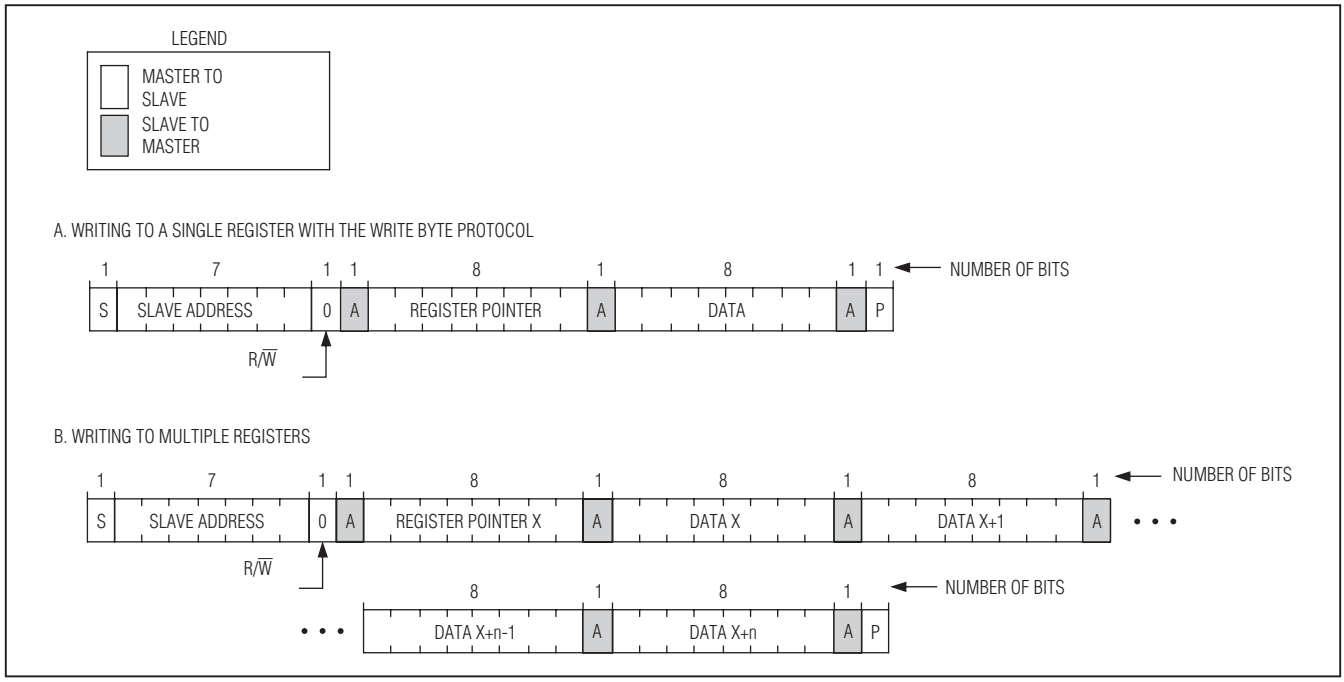


Figure 12. Writing to the MAX8893A/MAX8893B/MAX8893C

Read Operation

The method for reading a single register (byte) is shown in section A of Figure 13. To read a single register:

1) The master sends a start command.
2) The master sends the 7-bit slave address followed by a read bit (0x7D).
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer.
5) The slave acknowledges the register pointer.
6) The master sends a REPEATED START condition.
7) The master sends the 7-bit slave address followed by a read bit.
8) The slave asserts an acknowledge by pulling SDA low.
9) The slave sends the 8-bit data (contents of the register).
10) The master asserts an acknowledge by pulling SDA low.
11) The master sends a STOP condition.

In addition, the MAX8893A/MAX8893B/MAX8893C can read a block of multiple sequential registers as shown in section B of Figure 13. Use the following procedure to read a sequential block of registers:

1) The master sends a start command.
2) The master sends the 7-bit slave address followed by a read bit (0x7D).
3) The addressed slave asserts an acknowledge by pulling SDA low.
4) The master sends an 8-bit register pointer of the first register in the block.
5) The slave acknowledges the register pointer.
6) The master sends a REPEATED START condition.
7) The master sends the 7-bit slave address followed by a read bit.
8) The slave asserts an acknowledge by pulling SDA low.
9) The slave sends the 8-bit data (contents of the register).
10) The master asserts an acknowledge by pulling SDA low.
11) Steps 9 and 10 are repeated for as many registers in the block, with the register pointer automatically incremented each time.
12) The master sends a STOP condition.

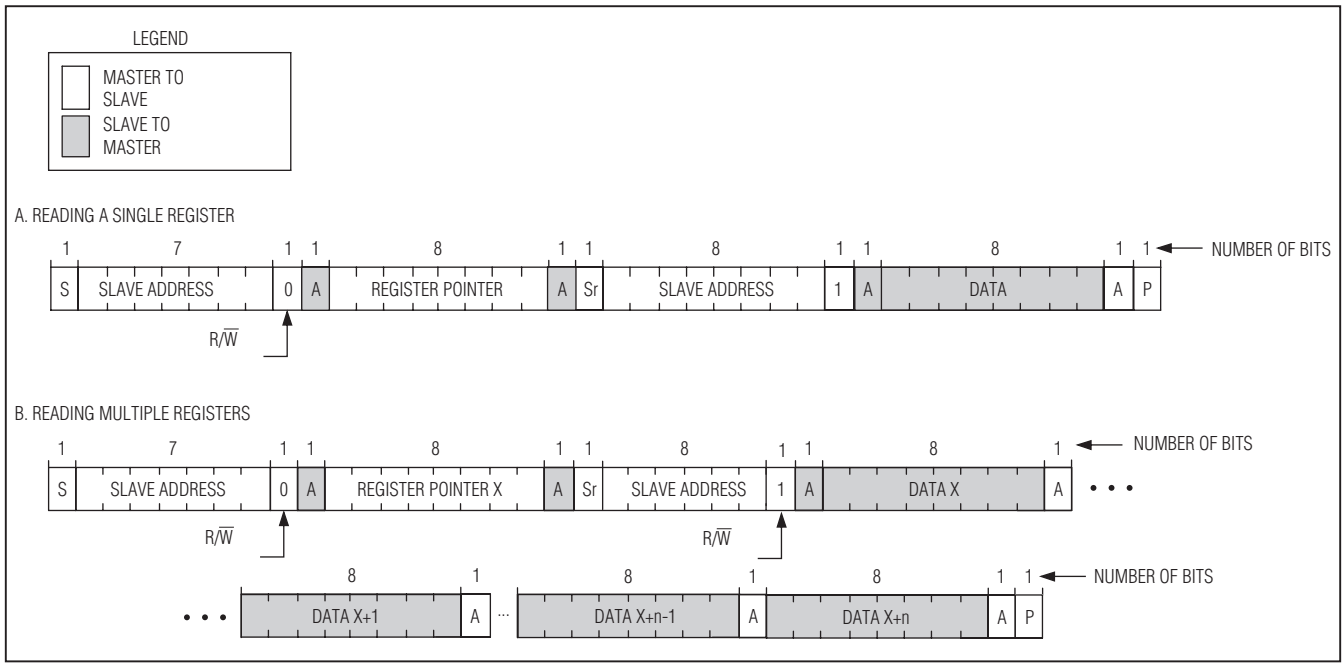


Figure 13. Reading from the MAX8893A/MAX8893B/MAX8893C

Table 5. Register Map

NAME	TABLE	REGISTER ADDRESS (hex)	RESET VALUE	TYPE	DESCRIPTION
ON/OFF CONTROL	Table 6	0x00	0x01	R/W	BUCK, LDO1–LDO5, load switch, and USB switch ON/OFF control
ACTIVE DISCHARGE CONTROL	Table 7	0x01	0xFF	R/W	Active discharge enable/disable control for step-down converter and LDO regulators
LS TIME CONTROL	Table 8	0x02	0x08	R/W	Load switch rising time, turn-on, and turn-off delay time control
DVS RAMP CONTROL	Table 9	0x03	0x09	R/W	BUCK enable and ramp rate control
BUCK	Table 10	0x04	0x02	R/W	BUCK output voltage setting
LDO1	Table 11	0x05	0x0C 0x0A 0x02	R/W	LDO1 output voltage setting
LDO2	Table 12	0x06	0x0E	R/W	LDO2 output voltage setting
LDO3	Table 13	0x07	0x11	R/W	LDO3 output voltage setting
LDO4	Table 14	0x08	0x16 0x19	R/W	LDO4 output voltage setting
LDO5	Table 15	0x09	0x02 0x14 0x16	R/W	LDO5 output voltage setting
SVER	Table 16	0x46	N/A	R only	Die type information

Table 6. On/Off Control

This register contains BUCK, LDO1–LDO5, USB switch, and load switch ON/OFF controls.

REGISTER NAME	ON/OFF CONTROL
Register Pointer	0x00
Reset Value	0x01
Type	Read/write
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	EBUCK	0 = BUCK is disabled 1 = BUCK is enabled	0
B6	ELS	0 = Load switch is disabled 1 = Load switch is enabled	0
B5	ELDO1	0 = LDO1 is disabled 1 = LDO1 is enabled	0
B4	ELDO2	0 = LDO2 is disabled 1 = LDO2 is enabled	0
B3	ELDO3	0 = LDO3 is disabled 1 = LDO3 is enabled	0
B2	ELDO4	0 = LDO4 is disabled 1 = LDO4 is enabled	0
B1	ELDO5	0 = LDO5 is disabled 1 = LDO5 is enabled	0
B0 (LSB)	$\overline{\text{EUSB}}$	0 = USB switch is enabled 1 = USB switch is disabled	1

Table 7. Active Discharge Control

This register contains the active discharge enable bits for the BUCK, load switch, and LDO1–LDO5.

REGISTER NAME	ACTIVE DISCHARGE CONTROL
Register Pointer	0x01
Reset Value	0xFF
Type	Read/write
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	BUCK_ADEN	0 = BUCK active discharge is disabled 1 = BUCK active discharge is enabled	1
B6	LS_ADEN	0 = Load switch active discharge is disabled 1 = Load switch active discharge is enabled	1
B5	LDO1_ADEN	0 = LDO1 active discharge is disabled 1 = LDO1 active discharge is enabled	1
B4	LDO2_ADEN	0 = LDO2 active discharge is disabled 1 = LDO2 active discharge is enabled	1
B3	LDO3_ADEN	0 = LDO3 active discharge is disabled 1 = LDO3 active discharge is enabled	1
B2	LDO4_ADEN	0 = LDO4 active discharge is disabled 1 = LDO4 active discharge is enabled	1
B1	LDO5_ADEN	0 = LDO5 active discharge is disabled 1 = LDO5 active discharge is enabled	1
B0 (LSB)	—	Reserved for future use	—

Table 8. LS Time Control

This register contains the load switch timing controls.

REGISTER NAME	LS TIME CONTROL
Register Pointer	0x02
Reset Value	0x08
Type	Read/write
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	—	Reserved for future use	—
B6	—	Reserved for future use	—
B5	—	Reserved for future use	—
B4	LSRT	Load switch rising time control 00 = 10µs 01 = 27µs 10 = 100µs 11 = 300µs	01
B3			
B2	LSTOD	Load switch turn-on delay time control 0 = Load switch turn-on delay OFF 1 = Load switch turn-on delay is 34µs	0
B1	LSTOFFD	Load switch turn-off delay time control 00 = 11µs 01 = 63µs 10 = 177µs 11 = 11µs	00
B0 (LSB)			

Table 9. DVS Ramp Control

This register contains DVS enable/disable and ramp rate control for the step-down converter.

REGISTER NAME	DVS RAMP CONTROL
Register Pointer	0x03
Reset Value	0x09
Type	Read/write
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	—	Reserved for future use	—
B6	—	Reserved for future use	—
B5	—	Reserved for future use	—
B4	ENDVS	0 = BUCK DVS is disabled 1 = BUCK DVS is enabled	0
B3	BUCKRAMP	Step-down output voltage ramp rate control 0000 (0x0) = 1mV/µs 0001 (0x1) = 2mV/µs 0010 (0x2) = 3mV/µs 0011 (0x3) = 4mV/µs 0100 (0x4) = 5mV/µs 0101 (0x5) = 6mV/µs 0110 (0x6) = 7mV/µs 0111 (0x7) = 8mV/µs 1000 (0x8) = 9mV/µs 1001 (0x9) = 10mV/µs 1010 (0xA) = 11mV/µs 1011 (0xB) = 12mV/µs	1001 (0x9)
B2			
B1			
B0 (LSB)			

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Table 10. Buck

This register contains the step-down converter output voltage controls.

REGISTER NAME	BUCK
Register Pointer	0x04
Reset Value	0x02
Type	Read/write
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	BUCK	00000000 (0x00) = 0.8V 00000001 (0x01) = 0.9V 00000010 (0x02) = 1.0V 00000011 (0x03) = 1.1V 00000100 (0x04) = 1.2V 00000101 (0x05) = 1.3V 00000110 (0x06) = 1.4V 00000111 (0x07) = 1.5V 00001000 (0x08) = 1.6V 00001001 (0x09) = 1.7V 00001010 (0x0A) = 1.8V 00001011 (0x0B) = 1.9V 00001100 (0x0C) = 2.0V 00001101 (0x0D) = 2.1V 00001110 (0x0E) = 2.2V 00001111 (0x0F) = 2.3V 00010000 (0x10) = 2.4V	00000010 (0x02)
B6			
B5			
B4			
B3			
B2			
B1			
B0 (LSB)			

Table 11. LDO1

This register contains LDO1 output voltage controls.

REGISTER NAME	ON/OFF CONTROL
Register Pointer	0x05
Reset Value	0x0C (MAX8893A) 0x0A (MAX8893B) 0x02 (MAX8893C)
Type	Read/write
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	LDO1	00000000 (0x00) = 1.6V 00000001 (0x01) = 1.7V 00000010 (0x02) = 1.8V 00000011 (0x03) = 1.9V 00000100 (0x04) = 2.0V 00000101 (0x05) = 2.1V 00000110 (0x06) = 2.2V 00000111 (0x07) = 2.3V 00001000 (0x08) = 2.4V 00001001 (0x09) = 2.5V 00001010 (0x0A) = 2.6V 00001011 (0x0B) = 2.7V 00001100 (0x0C) = 2.8V 00001101 (0x0D) = 2.9V 00001110 (0x0E) = 3.0V 00001111 (0x0F) = 3.1V 00010000 (0x10) = 3.2V 00010001 (0x11) = 3.3V	MAX8893A 00001100 (0x0C) MAX8893B 00001010 (0x0A) MAX8893C 00000010 (0x02)
B6			
B5			
B4			
B3			
B2			
B1			
B0 (LSB)			

Table 12. LDO2

This register contains LDO2 output voltage controls.

REGISTER NAME	LDO2
Register Pointer	0x06
Reset Value	0x0E
Type	Read/write
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	LDO2	00000000 (0x00) = 1.2V 00000001 (0x01) = 1.3V 00000010 (0x02) = 1.4V 00000011 (0x03) = 1.5V 00000100 (0x04) = 1.6V 00000101 (0x05) = 1.7V 00000110 (0x06) = 1.8V 00000111 (0x07) = 1.9V 00001000 (0x08) = 2.0V 00001001 (0x09) = 2.1V 00001010 (0x0A) = 2.2V 00001011 (0x0B) = 2.3V 00001100 (0x0C) = 2.4V 00001101 (0x0D) = 2.5V 00001110 (0x0E) = 2.6V 00001111 (0x0F) = 2.7V 00010000 (0x10) = 2.8V 00010001 (0x11) = 2.9V 00010010 (0x12) = 3.0V 00010011 (0x13) = 3.1V 00010100 (0x14) = 3.2V 00010101 (0x15) = 3.3V	00001110 (0x0E)
B6			
B5			
B4			
B3			
B2			
B1			
B0 (LSB)			

Table 13. LDO3

This register contains LDO3 output voltage controls.

REGISTER NAME	LDO3
Register Pointer	0x07
Reset Value	0x11
Type	Read/write
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	LDO3	00000000 (0x00) = 1.6V 00000001 (0x01) = 1.7V 00000010 (0x02) = 1.8V 00000011 (0x03) = 1.9V 00000100 (0x04) = 2.0V 00000101 (0x05) = 2.1V 00000110 (0x06) = 2.2V 00000111 (0x07) = 2.3V 00001000 (0x08) = 2.4V 00001001 (0x09) = 2.5V 00001010 (0x0A) = 2.6V 00001011 (0x0B) = 2.7V 00001100 (0x0C) = 2.8V 00001101 (0x0D) = 2.9V 00001110 (0x0E) = 3.0V 00001111 (0x0F) = 3.1V 00010000 (0x10) = 3.2V 00010001 (0x11) = 3.3V	00010001 (0x11)
B6			
B5			
B4			
B3			
B2			
B1			
B0 (LSB)			

Table 14. LDO4

This register contains LDO4 output voltage controls.

REGISTER NAME	LDO4
Register Pointer	0x08
Reset Value	0x16(MAX8893A) 0x19(MAX8893B/MAX8893C)
Type	Read/write
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	LDO4	00000000 (0x00) = 0.8V 00000001 (0x01) = 0.9V 00000010 (0x02) = 1.0V 00000011 (0x03) = 1.1V 00000100 (0x04) = 1.2V 00000101 (0x05) = 1.3V 00000110 (0x06) = 1.4V 00000111 (0x07) = 1.5V 00001000 (0x08) = 1.6V 00001001 (0x09) = 1.7V 00001010 (0x0A) = 1.8V 00001011 (0x0B) = 1.9V 00001100 (0x0C) = 2.0V 00001101 (0x0D) = 2.1V 00001110 (0x0E) = 2.2V 00001111 (0x0F) = 2.3V 00010000 (0x10) = 2.4V 00010001 (0x11) = 2.5V 00010010 (0x12) = 2.6V 00010011 (0x13) = 2.7V 00010100 (0x14) = 2.8V 00010101 (0x15) = 2.9V 00010110 (0x16) = 3.0V 00010111 (0x17) = 3.1V 00011000 (0x18) = 3.2V 00011001 (0x19) = 3.3V	MAX8893A 00010110 (0x16) MAX8893B /MAX8893C 00011001 (0x19)
B6			
B5			
B4			
B3			
B2			
B1			
B0 (LSB)			

Table 15. LDO5

This register contains LDO5 output voltage controls.

REGISTER NAME	LDO5
Register Pointer	0x09
Reset Value	0x02 (MAX8893A) 0x14 (MAX8893B) 0x16 (MAX8893C)
Type	Read/write
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB) B6 B5 B4 B3 B2 B1 B0 (LSB)	LDO5	00000000 (0x00) = 0.8V 00000001 (0x01) = 0.9V 00000010 (0x02) = 1.0V 00000011 (0x03) = 1.1V 00000100 (0x04) = 1.2V 00000101 (0x05) = 1.3V 00000110 (0x06) = 1.4V 00000111 (0x07) = 1.5V 00001000 (0x08) = 1.6V 00001001 (0x09) = 1.7V 00001010 (0x0A) = 1.8V 00001011 (0x0B) = 1.9V 00001100 (0x0C) = 2.0V 00001101 (0x0D) = 2.1V 00001110 (0x0E) = 2.2V 00001111 (0x0F) = 2.3V 00010000 (0x10) = 2.4V 00010001 (0x11) = 2.5V 00010010 (0x12) = 2.6V 00010011 (0x13) = 2.7V 00010100 (0x14) = 2.8V 00010101 (0x15) = 2.9V 00010110 (0x16) = 3.0V 00010111 (0x17) = 3.1V 00011000 (0x18) = 3.2V 00011001 (0x19) = 3.3V	MAX8893A 00000010 (0x02) MAX8893B 00010100 (0x14) MAX8893C 00010110 (0x16)

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Table 16. SVER

This register contains the MAX8893A/MAX8893B/MAX8893C version number.

REGISTER NAME	SVER
Register Pointer	0x46
Reset Value	N/A
Type	Read
Special Features	—

BIT	NAME	DESCRIPTION	DEFAULT VALUE
B7 (MSB)	—	Reserved for future use	—
B6	—	Reserved for future use	—
B5	—	Reserved for future use	—
B4	—	Reserved for future use	—
B3	—	Reserved for future use	—
B2	—	Reserved for future use	—
B1	SVER	00 = MAX8893A 01 = MAX8893B 10 = MAX8893C	—
B0 (LSB)			

Applications Information

Step-Down Converter

Input Capacitor

The input capacitor, C_{IN1}, reduces the current peaks drawn from the battery or input power source and reduces switching noise in the IC. The impedance of C_{IN1} at the switching frequency should be kept very low. Ceramic capacitors with X5R or X7R temperature characteristics are highly recommended due to their small size, low ESR, and small temperature coefficients. Due to the step-down converter's fast soft-start, the input capacitance can be very low. For most applications, a 2.2µF capacitor is sufficient. Connect C_{IN1} as close as possible to the IC to minimize the impact of PCB trace inductance.

For other input capacitors, use a 2.2µF ceramic capacitor from IN2 to ground and a 2.2µF ceramic capacitor from BATT to ground.

Output Capacitor

The output capacitor, C_{BUCK}, is required to keep the output voltage ripple small and to ensure regulation loop stability. C_{BUCK} must have low impedance at the switching frequency. Ceramic capacitors with X5R or X7R temperature characteristics are highly recommended due to their small size, low ESR, and small temperature coefficients. Due to the unique feedback network, the output capacitance can be very low. For most applications a 2.2µF capacitor is sufficient. For optimum load-transient performance and very low output ripple, the output capacitor value in µF should be equal to or larger than the inductor value in µH.

Inductor Selection

The recommended inductor for the step-down converter is from 1.0µH and 4.7µH. Low inductance values are physically smaller, but require faster switching, resulting in some efficiency loss. The inductor's DC current rating needs to be only 100mA greater than the application's maximum load current because the step-down converter features zero current overshoot during startup and load transients.

For output voltages above 2.0V, when light load efficiency is important, the minimum recommended inductor is 2.2µH. For optimum voltage-positioning load transients, choose an inductor with DC series resistance in the 50mΩ to 150mΩ range. To achieve higher efficiency at heavy loads (above 200mA) or minimum load regulation (but some transient overshoot), the inductor resistance should be kept below 100mΩ. For light -oad applications up to 200mA, much higher resistance is acceptable with very little impact on performance. See Table 17 for some suggested inductors.

Table 17. Suggested Inductors

MANUFACTURER	SERIES	INDUCTANCE (µH)	ESR (mΩ)	ISAT (mA)	DIMENSIONS (L_{TYP} x W_{TYP} x H_{MAX}) (mm)
Taiyo Yuden	LB2012	1.0 2.2	150 230	300 240	2.0 x 1.25 x 1.45
	LB2016	1.0 1.5 2.2 3.3	90 110 130 200	455 350 315 280	2.0 x 1.6 x 1.8
	LB2518	1.0 1.5 2.2 3.3	60 70 90 110	500 400 340 270	2.5 x 1.8 x 2.0
	LBC2518	1.0 1.5 2.2 3.3 4.7	80 110 130 160 200	775 660 600 500 430	2.5 x 1.8 x 2.0
Murata	LQH32C_53	1.0 2.2 4.7	60 100 150	1000 790 650	3.2 x 2.5 x 1.7
	LQM43FN	2.2 4.7	100 170	400 300	4.5 x 3.2 x 0.9
TOKO	D310F	1.5 2.2 3.3	130 170 190	1230 1080 1010	3.6 x 3.6 x 1.0
	D312C	1.5 2.2 2.7 3.3	100 120 150 170	1290 1140 980 900	3.6 x 3.6 x 1.2
Sumida	CDRH2D11	1.5 2.2 3.3 4.7	50 80 100 140	900 780 600 500	3.2 x 3.2 x 1.2

FPMIC for Multimedia Application Processor in 2.5mm x 3.0mm WLP

Capacitors for LDOs

For LDOs, the required output capacitance is dependent on the load currents. With rated maximum load currents, 2.2µF (typ) capacitors are recommended for LDO1, LDO2, LDO3, and LDO5 and a 1.0µF capacitor is recommended for LDO4. For loads less than 150mA, it is sufficient to use 1.0µF capacitors for stable operation over the full temperature range for LDO1, LDO2, LDO3, and LDO5. Reduce output noise and improve load transient response, stability, and power-supply rejection by using larger output capacitors.

USB High-Speed Switch

USB Switching

The USB high-speed switch is fully compliant with the USB 2.0 specification. The low on-resistance and low on-capacitance of these switches make it ideal for high-performance switching applications. It is ideal for routing USB data lines (see Figure 14) and for applications that require switching between multiple USB hosts (see Figure 15). The USB switch also features overvoltage fault protection to guard systems against shorts to the USB VBUS voltage that is required for all USB applications.

Extended ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. COM1 and COM2 are further protected against static electricity. The state-of-the-art structures are developed to protect these pins against ESD up to ±15kV without damage. The ESD structures withstand high ESD in normal operation and when the device is powered down. After an ESD event, the USB switch continues to function without latchup.

The USB high-speed switch is characterized for protection to the following limits:

- ±15kV using Human Body Model
- ±8kV using IEC 61000-4-2 Contact Discharge method
- ±15kV using IEC 61000-4-2 Air-Gap Discharge method

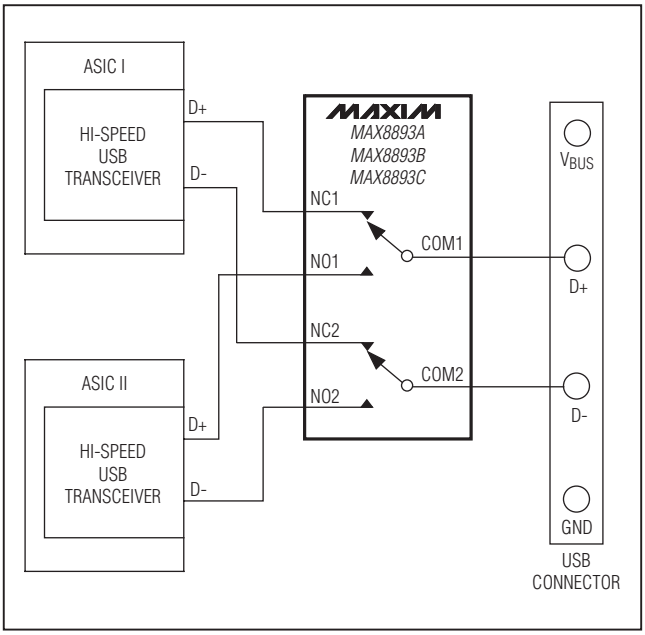


Figure 14. USB Data Routing/Typical Application Circuit

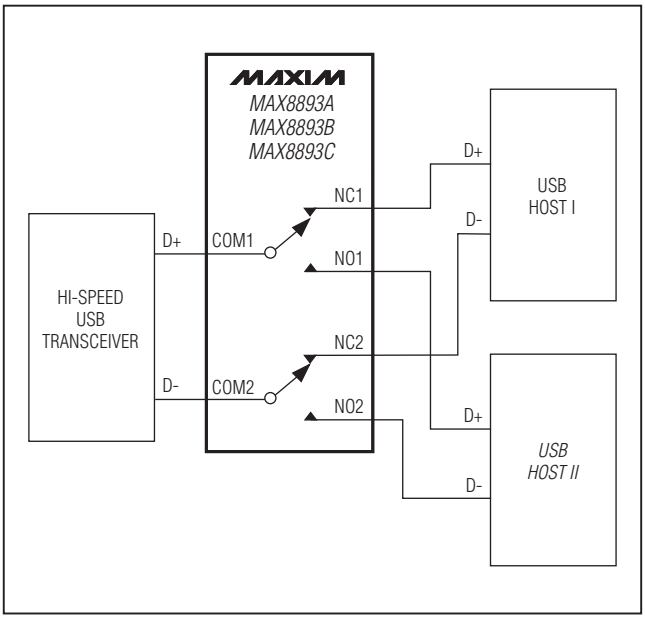


Figure 15. Switching Between Multiple USB Hosts

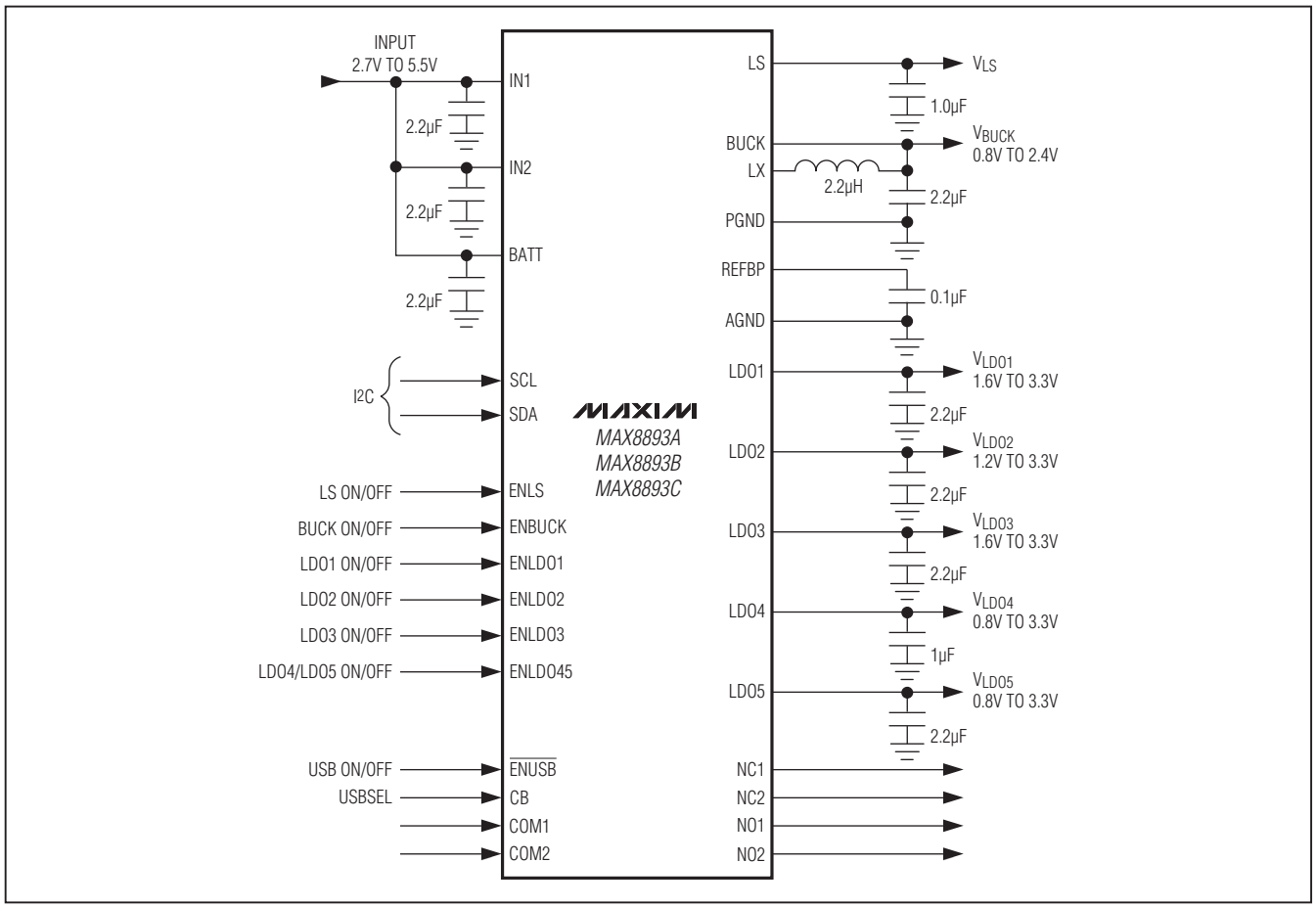
PCB Layout and Routing

High switching frequencies and relatively large peak currents make the PCB layout a very important aspect of design. Good design minimizes excessive EMI on the voltage gradients in the ground plane that can result in instability or regulation errors. Connect the input and output capacitors as close as possible to the IC. Connect the inductor as close as possible to the IC and keep the traces short, direct, and wide. Connect AGND to the exposed pad directly under the IC. Connect AGND and PGND to the ground plane. Keep noisy traces, such as the LX node, as short as possible.

USB Hi-Speed requires careful PCB layout with 45Ω controlled-impedance matched traces of equal lengths. Ensure that bypass capacitors are as close as possible to the IC. Use large ground planes where possible.

Refer to the MAX8893 evaluation kit for an example PCB layout design.

Typical Operating Circuit



µPMICs for Multimedia Application Processors in a 3.0mm x 2.5mm WLP

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
30 WLP	W302A3+2	21-0016

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/09	Initial release	—
1	2/10	Added new TOCs 53, 54, and 55 to *Typical Operating Characteristics* section	21